

COMPAL CONFIDENTIAL

MODEL NAME :
FDI40 N3-14", FDI4A V3-14", FDI43 N5-14",
FDI50 N3-15", FDI5A V3-15", FDI53 N5-15",
FDI70 N3-17"

PCB NO : DA60027S000 (SBD R)
DA60027S100 (NBDR)

BOM P/N :

SBDR-UMA	NBDR-UMA	X4E
431AJ331L51 431AJ331L54	431AJ331L01	X4E AJ331L51(N3)
431AJ331L52 431AJ331L55	431AJ331L02	X4E AJ331L52(V3)
431AJ331L53 431AJ331L56	431AJ331L03	X4E AJ331L01(N5)

CML-U+MEC1418
2019-06-19
REV : 1.0 (A00)

PCB R1

ZZZ PCB_FDI50_LA-G717P_LS-F112P/F114P/G711P	DAZ2QT00100 PCB_SBD R_R1@	ZZZ2 PCB_FDI53_LA-G717P_LS-G718P	DAZ2SO00100 PCB_NBRD_R1@
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PCB R3

ZZZ3 PCB_FDI50_LA-G717P_LS-F112P_GOLD A31 !	DAZ2QT00101 PCB_SBD R_R3_GCE@	ZZZ4 PCB_FDI53_LA-G717P_LS-G718P_GOLD A31 !	DAZ2SO00101 PCB_NBRD_R3_GCE@
ZZZ5 PCB_FDI50_LA-G717P_LS-F112P_TRIPOD A31 !	DAZ2QT00102 PCB_SBD R_R3_TRI@	ZZZ6 PCB_FDI53_LA-G717P_LS-G718P_TRIPOD A31 !	DAZ2SO00102 PCB_NBRD_R3_TRI@
ZZZ7 PCB_FDI50_LA-G717P_LS-F112P_HANN S A31 !	DAZ2QT00103 PCB_SBD R_R3_HAN@	ZZZ8 PCB_FDI53_LA-G717P_LS-G718P_HANN S A31 !	DAZ2SO00103 PCB_NBRD_R3_HAN@
ZZZ9 PCB_FDI50_LA-G717P_LS-F112P_T-MAC A31 !	DAZ2QT00104 PCB_SBD R_R3_TMT@	ZZZ10 PCB_FDI53_LA-G717P_LS-G718P_T-MAC A31 !	DAZ2SO00104 PCB_NBRD_R3_TMT@

CPU R1

UC12 S IC FJ8070104307606 SRGL0 V0 2.1G BGA	i3-10110U SA0000CU31L CML_2.1G_R1@
UC13 S IC FJ8070104307504 SRGKY V0 1.6G BGA	i5-10210U SA0000CST2L CML_1.6G_R1@
UC14 S IC FJ8070104303905 SRGKW V0 1.8G FCBGA	i7-10510U SA0000CU22L CML_1.8G_R1@

CPU R3

UC1 S IC FJ8070104307606 SRGL0 V0 2.1G A31 !	i3-10110U SA0000CU32L CML_2.1G_R3@
UC1 S IC FJ8070104307504 SRGKY V0 1.6G A31 !	i5-10210U SA0000CST3L CML_1.6G_R3@
UC1 S IC FJ8070104303905 SRGKW V0 1.8G A31 !	i7-10510U SA0000CU21L CML_1.8G_R3@

@ : Un-pop Component
DIS@ : GPU Support
N3@/V3@ : Inspiron/Vostro
CML@/CNL@ : CML/CNL
BASE@/PREM@ : (Pentium)(Celeron)i3 i5 i7


EC@ : EC Support
JP@/PJP@ : JUMP
100@/1000@: Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
750_CTPM@:750 and china TPM
ST_CTPM@:ST and china TPM
CTPM@:China TPM
FFS@ : Free Fall Sensor
TYPEC@ : TypeC
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component

PCB@/PCB_R1@/PCB_R3_G@/PCB_R3_T@/PCB_R3_H@/PCB_R3_TM@: PCB MB

PCB_NBRD_R1@: PCB MB for NBDR
TS_NON@/TS_USB@/TS_I2C@: Touch Screen Interface Select
SBD R@/NBDR@: SBD R/ NBDR Select

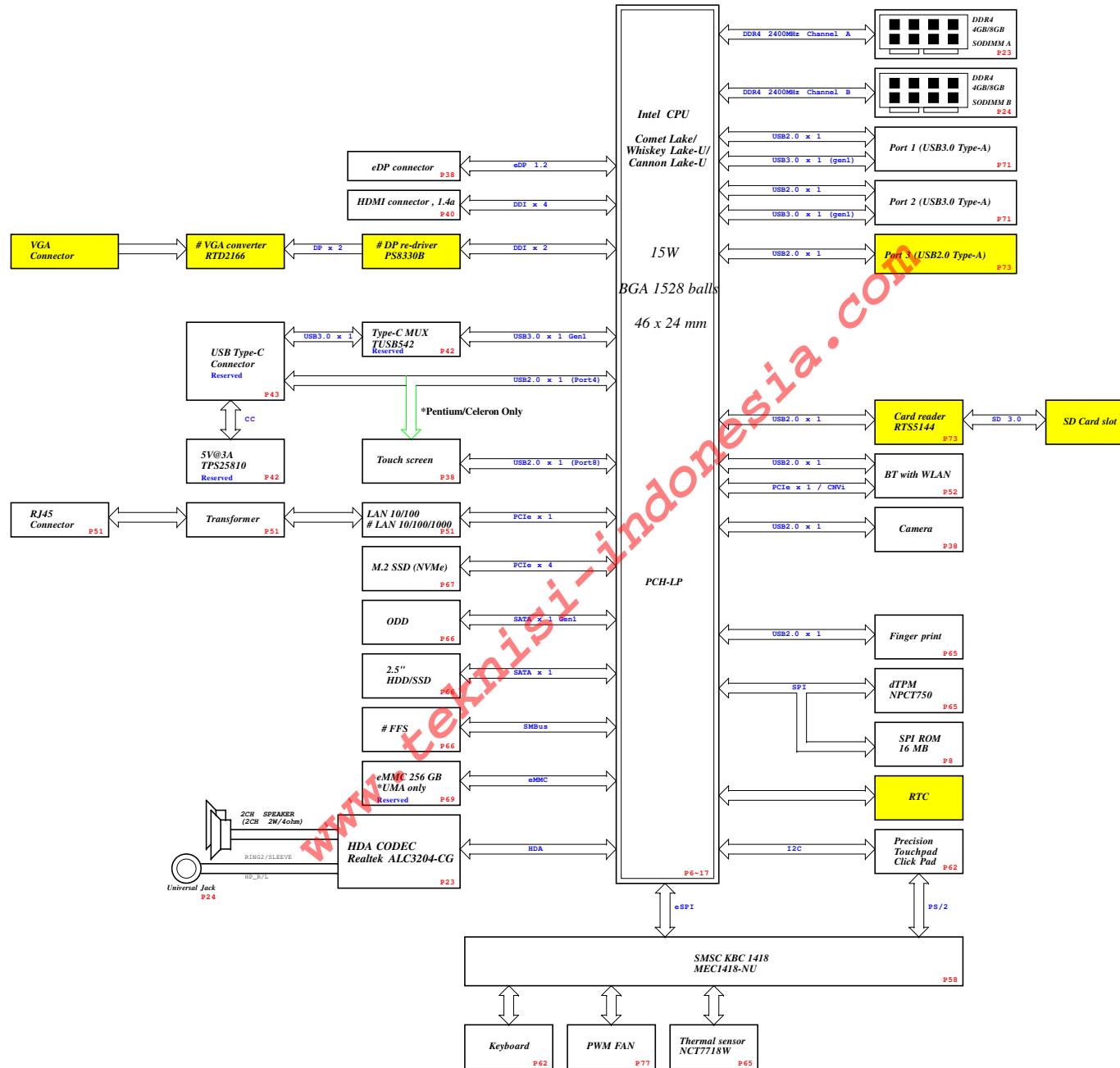
Layout Dell logo



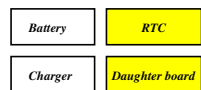
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Block Diagram



----> Loki-L only



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 Port, IO/B
4*	Touch screen
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Reserved
9	NA
10	BT

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 port1
USB3.0-2	PCIE-2		NA
USB3.0-3	PCIE-3		USB3.0 port2
USB3.0-4	PCIE-4		TypeC
USB3.0-5	PCIE-5		
USB3.0-6	PCIE-6		
	PCIE-7		
	PCIE-8		
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA ODD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

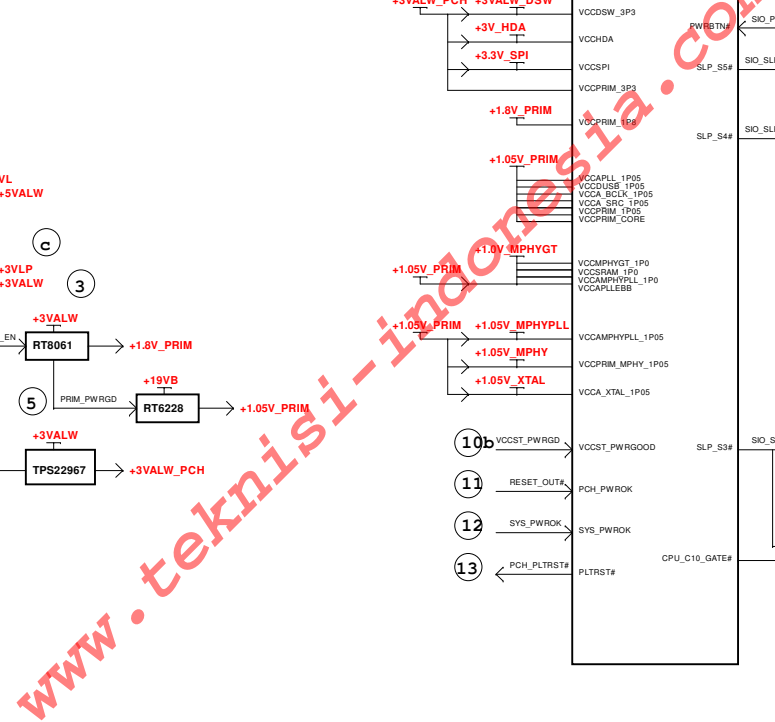
Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100	10.0	3.000	EVT	SBDR-UMA
2	100	17.8	2.801	DVT1	
3	100	27.0	2.598		NBDR-UMA
4	100	37.4	2.402	DVT2	
5	100	49.9	2.201		SBDR-DSC
6	100	64.9	2.001	Pilot	
7	100	82.5	1.808		NBDR-DSC
8	100	107.0	1.594		
9	100	154.0	1.299		
10	100	200.0	1.100		

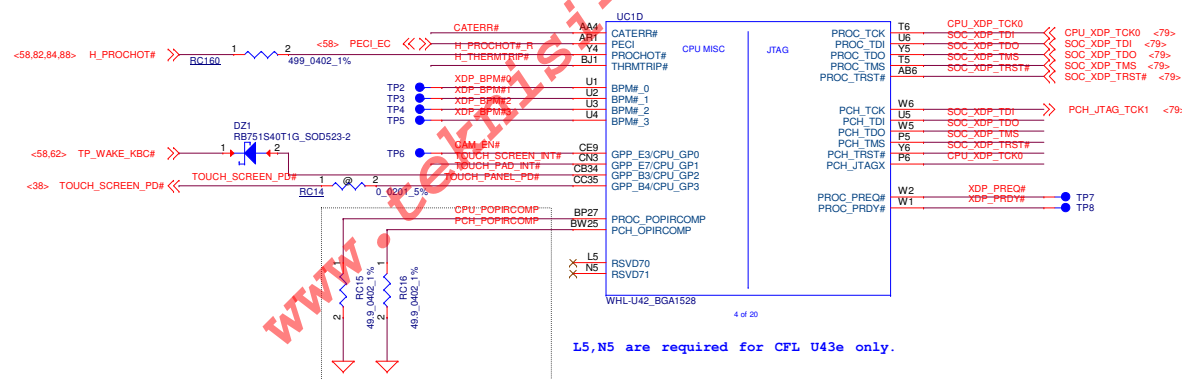
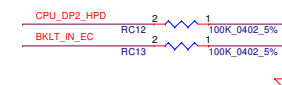
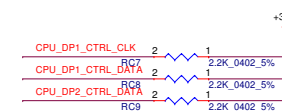
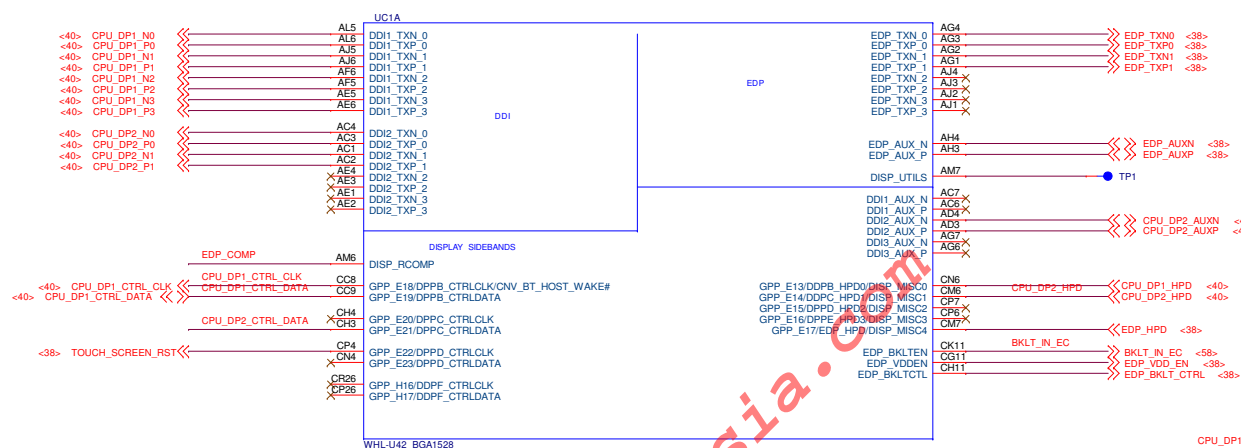
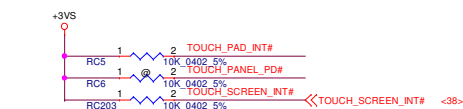
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support					No Support				Yes					Yes	

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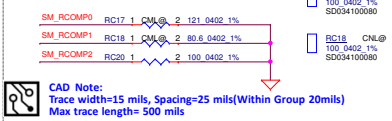


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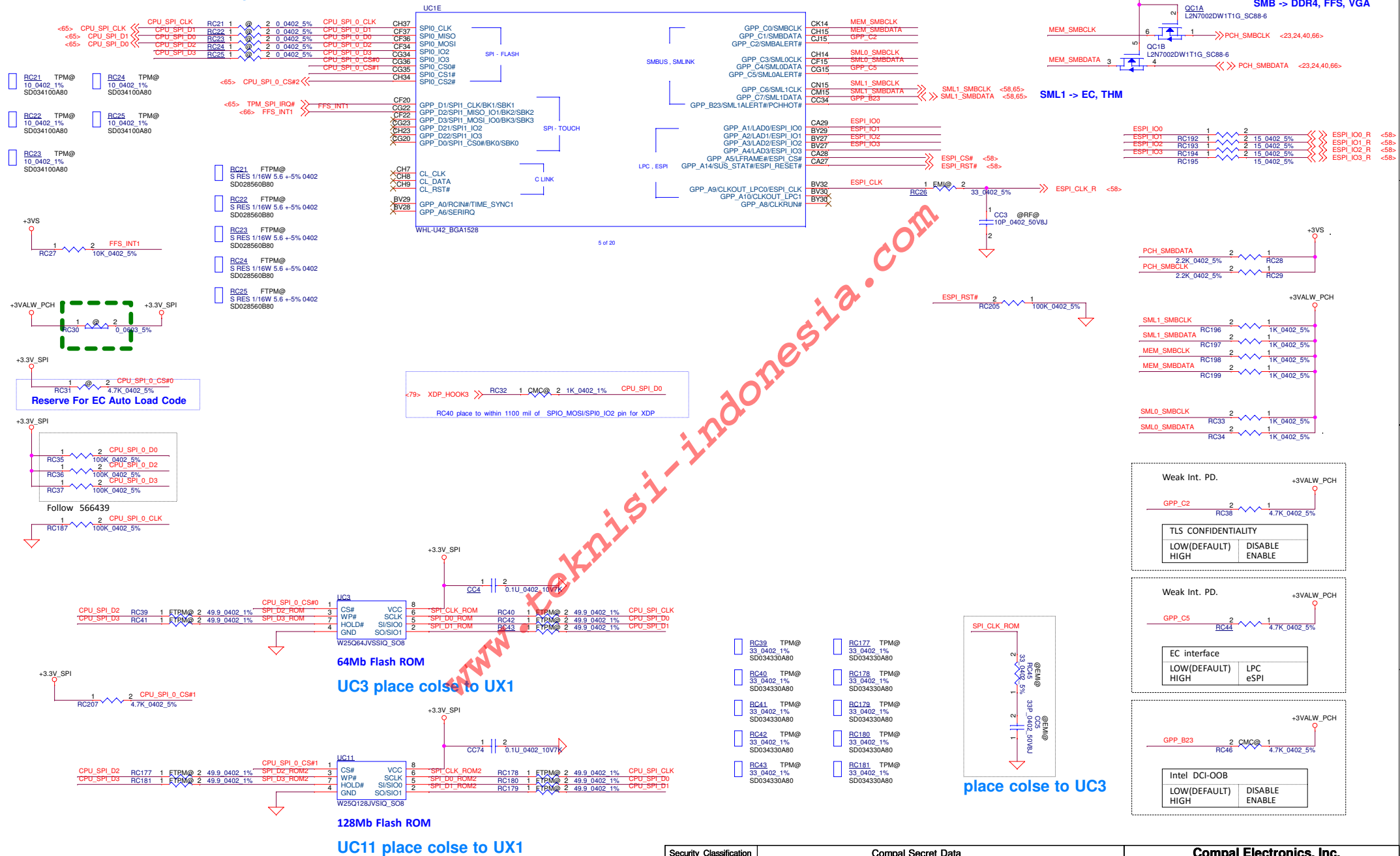
DDR4 Interleaved Memory



DDR4 COMPENSATION SIGNALS

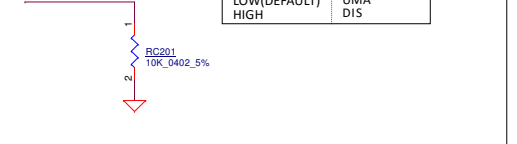
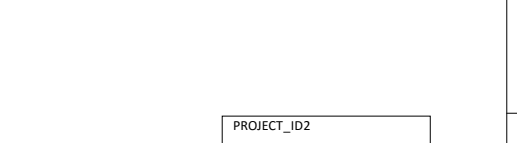
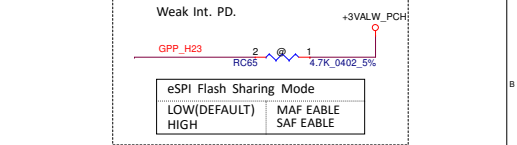
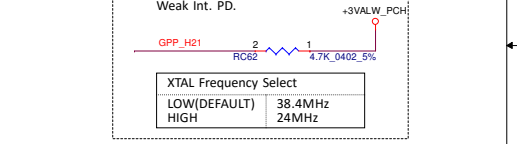
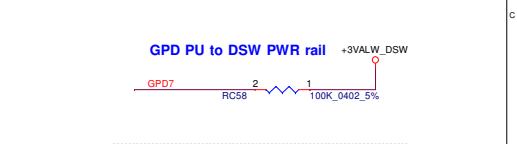
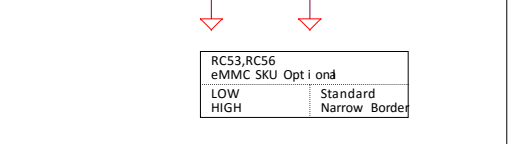
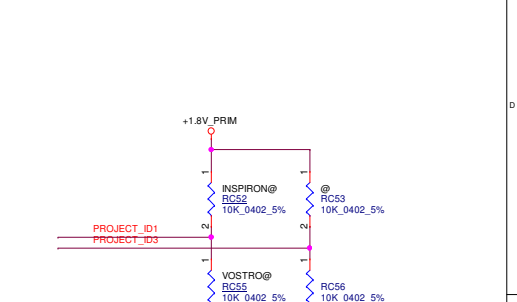
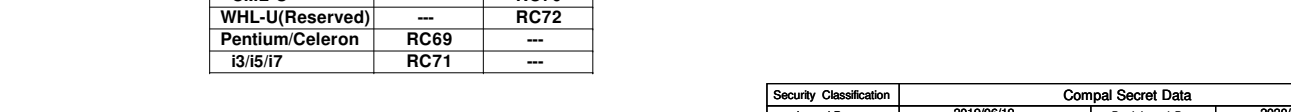
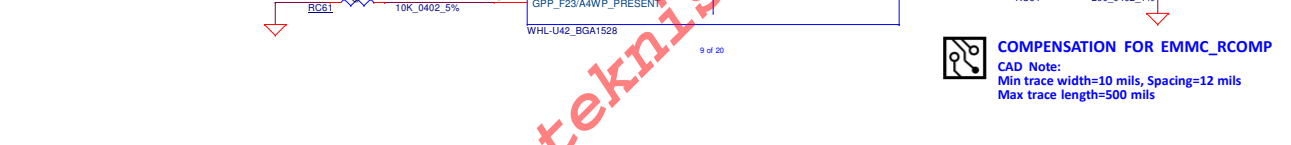
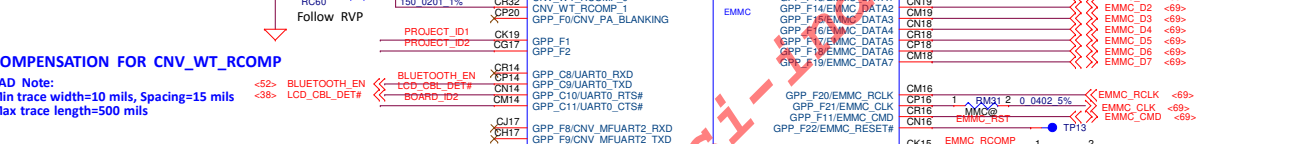
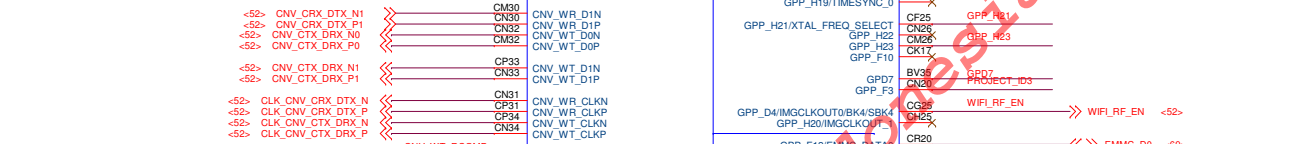
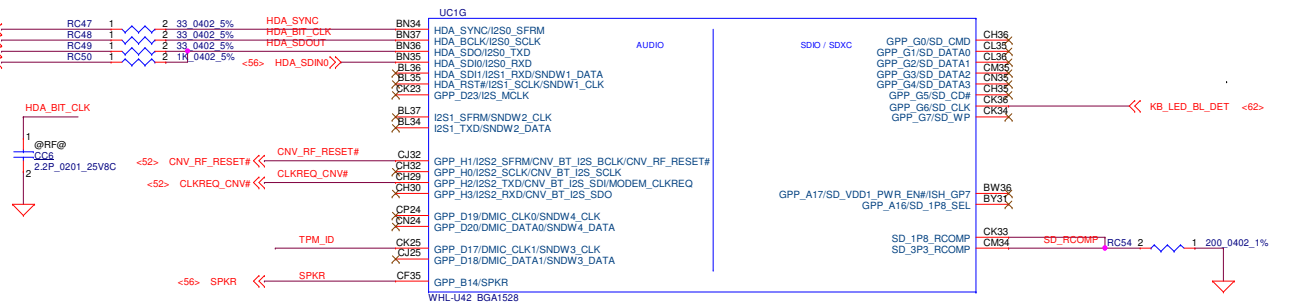
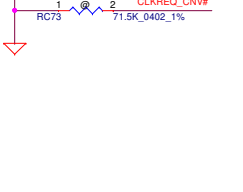
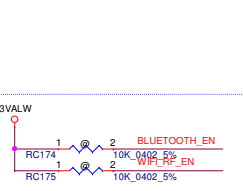
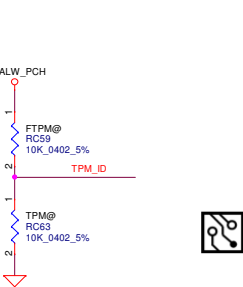
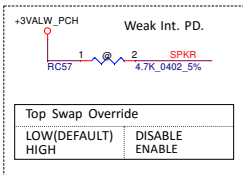
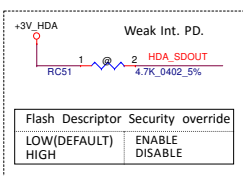
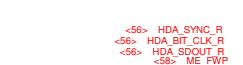


RC21~RC25 place colse to Device



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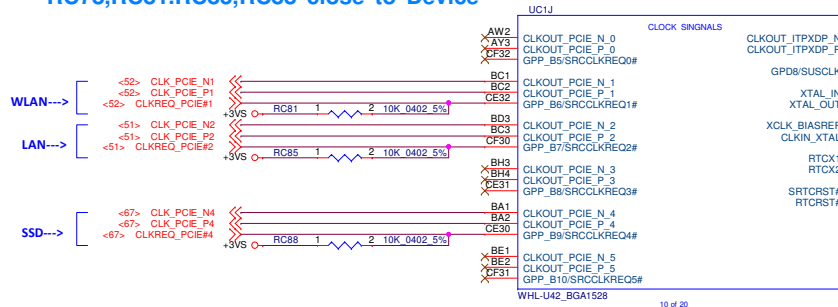
ME_FWP
LOW = ENABLE -->ME lock, can't update ME
HIGH = DISABLE -->ME un-lock, can update ME



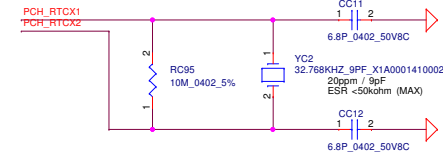
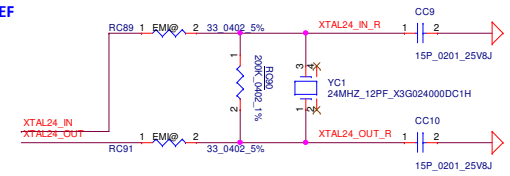
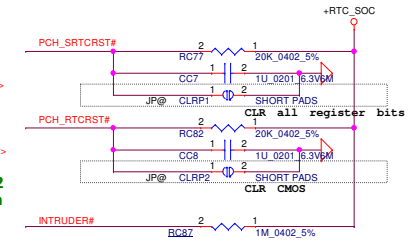
CPU ID	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
CML-U	---	RC70
WHL-U(Reserved)	---	RC72
Pentium/Celeron	RC69	---
i3/i5/i7	RC71	---

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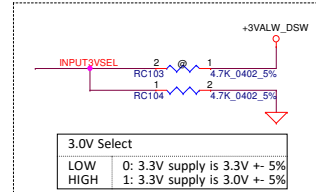
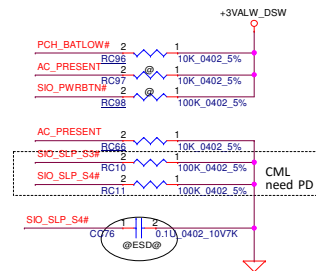
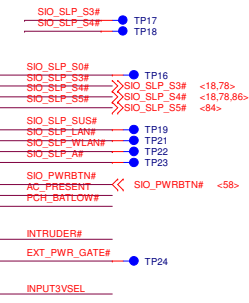
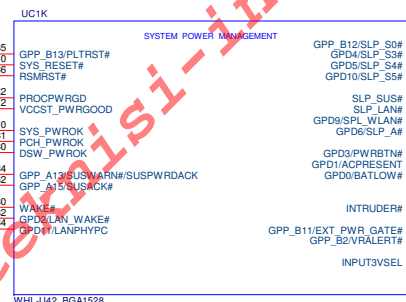
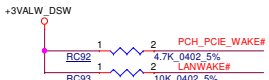
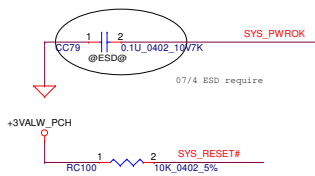
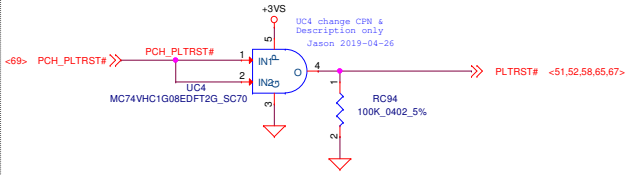
RC78,RC81,RC85,RC88 close to Device



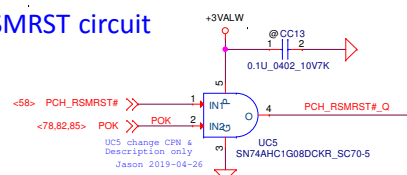
COMPENSATION FOR XCLK_BIASREF
CAD Note:
Min trace width=10 mils, Spacing=15 mils
Max trace length=1000 mils



PCH_PLTRST#



RSMRST circuit



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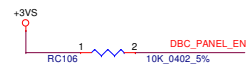
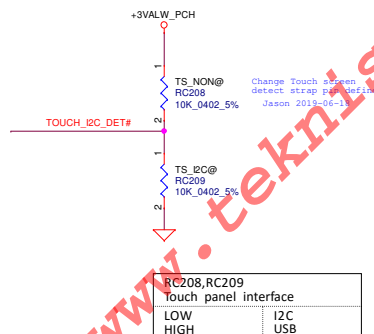
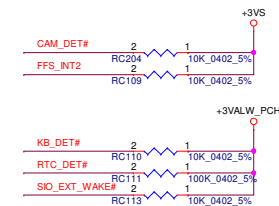
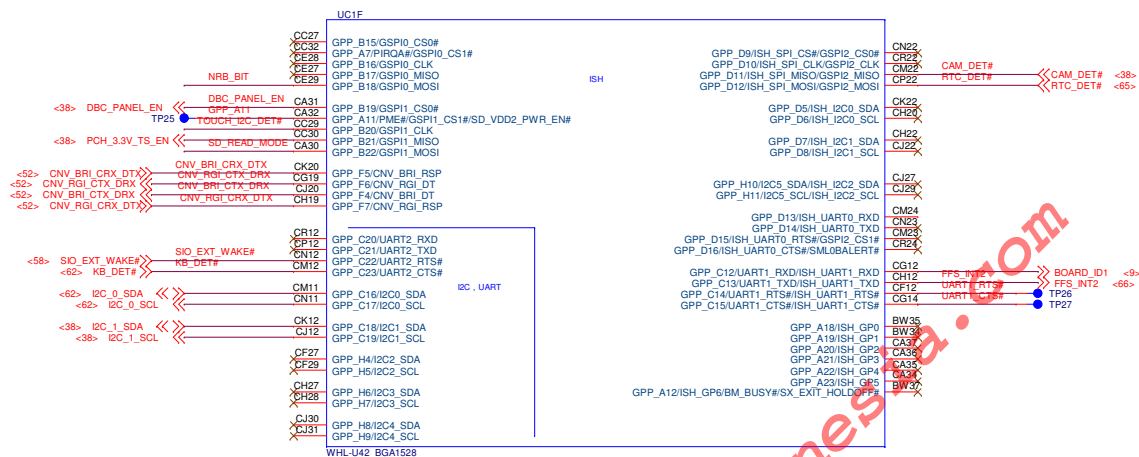
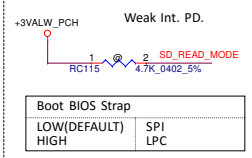
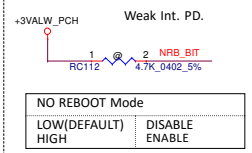


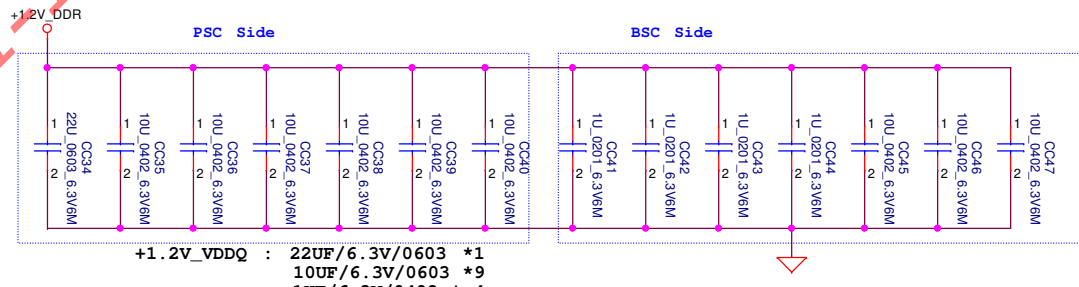
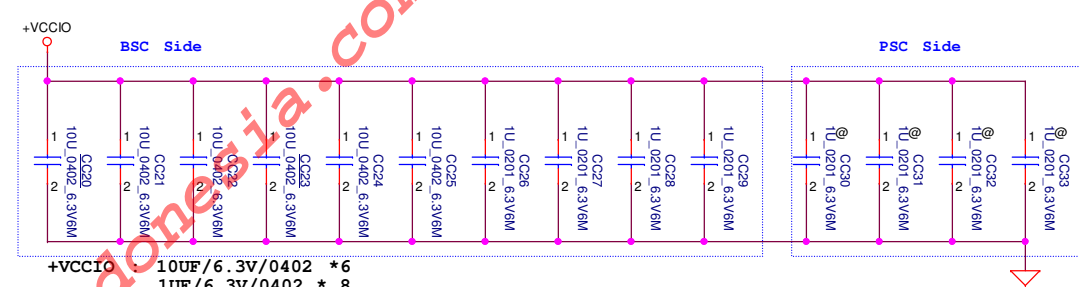
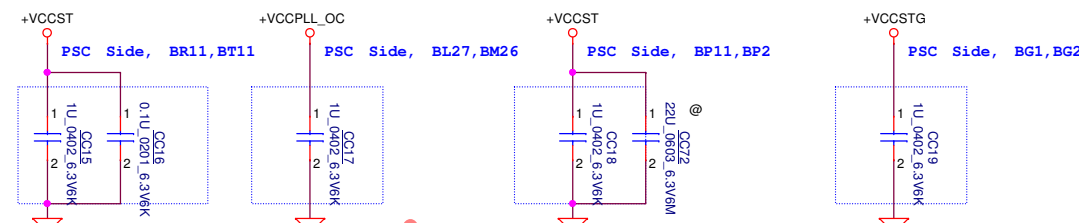
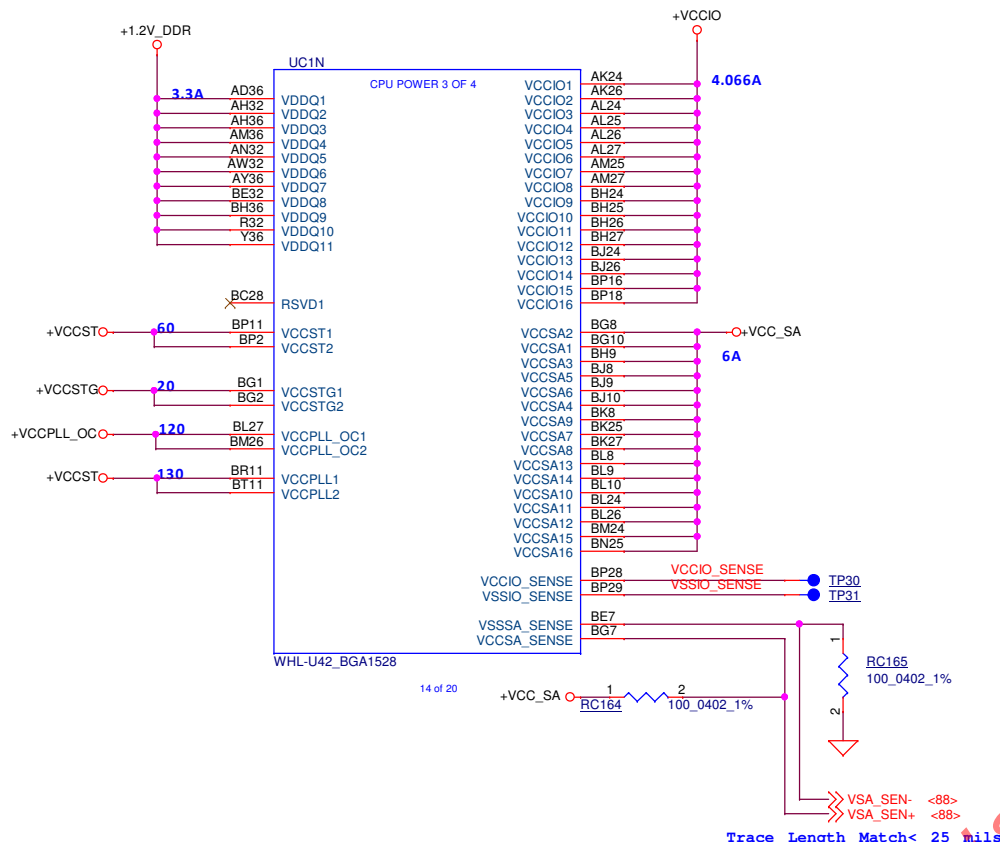
Diagram illustrating the M.2 CNV Mode Select circuit. The circuit is powered by +1.8V PRIM. The mode select is controlled by the CNV1 pin, which is connected to a network of resistors and capacitors. The output of this network is connected to the CNV_RGI_CTX_DRX pin.

M.2 CNV Mode Select	
LOW	CNV1 ENABLE
HIGH	CNV1 DISABLE



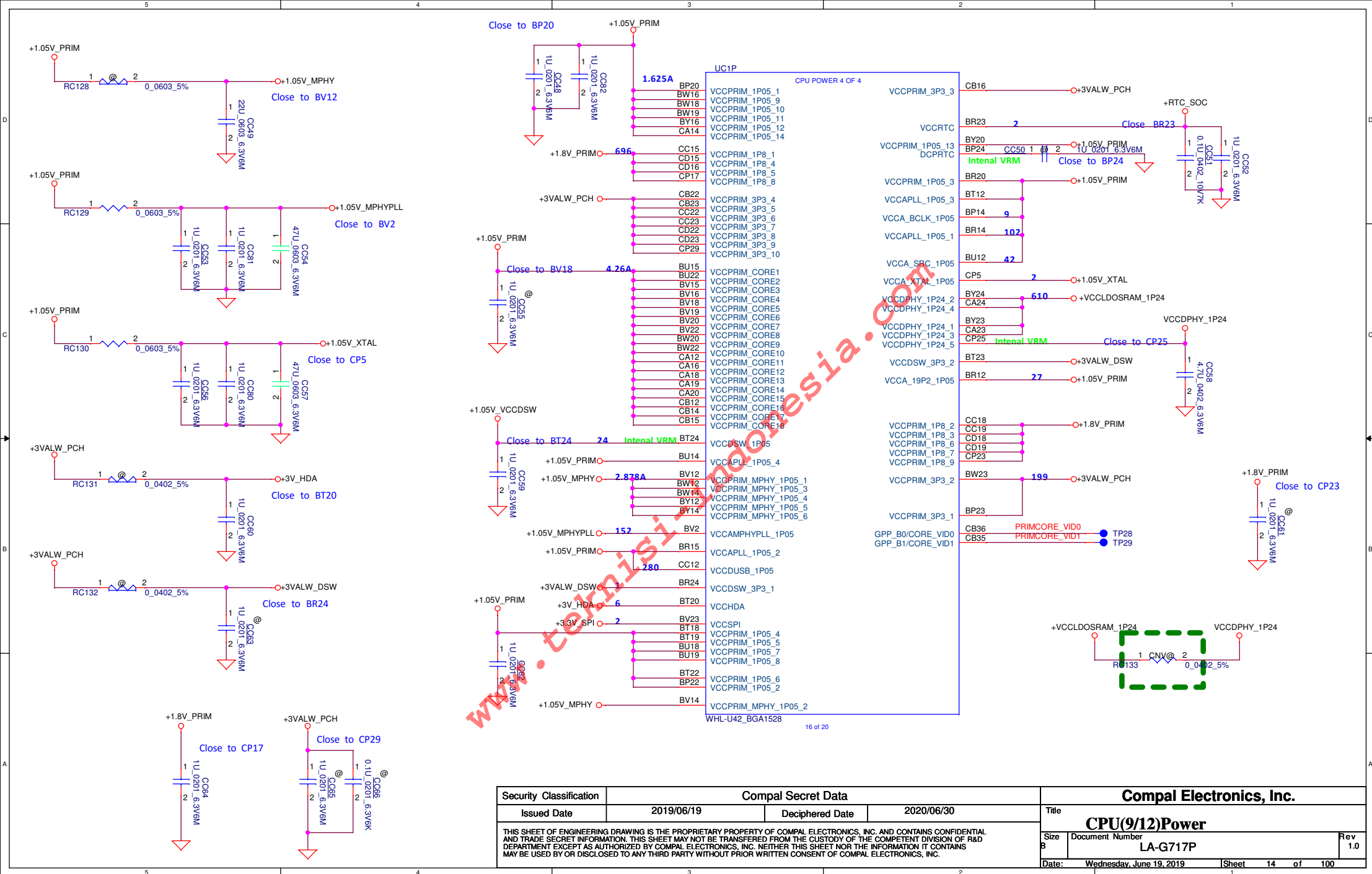
VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

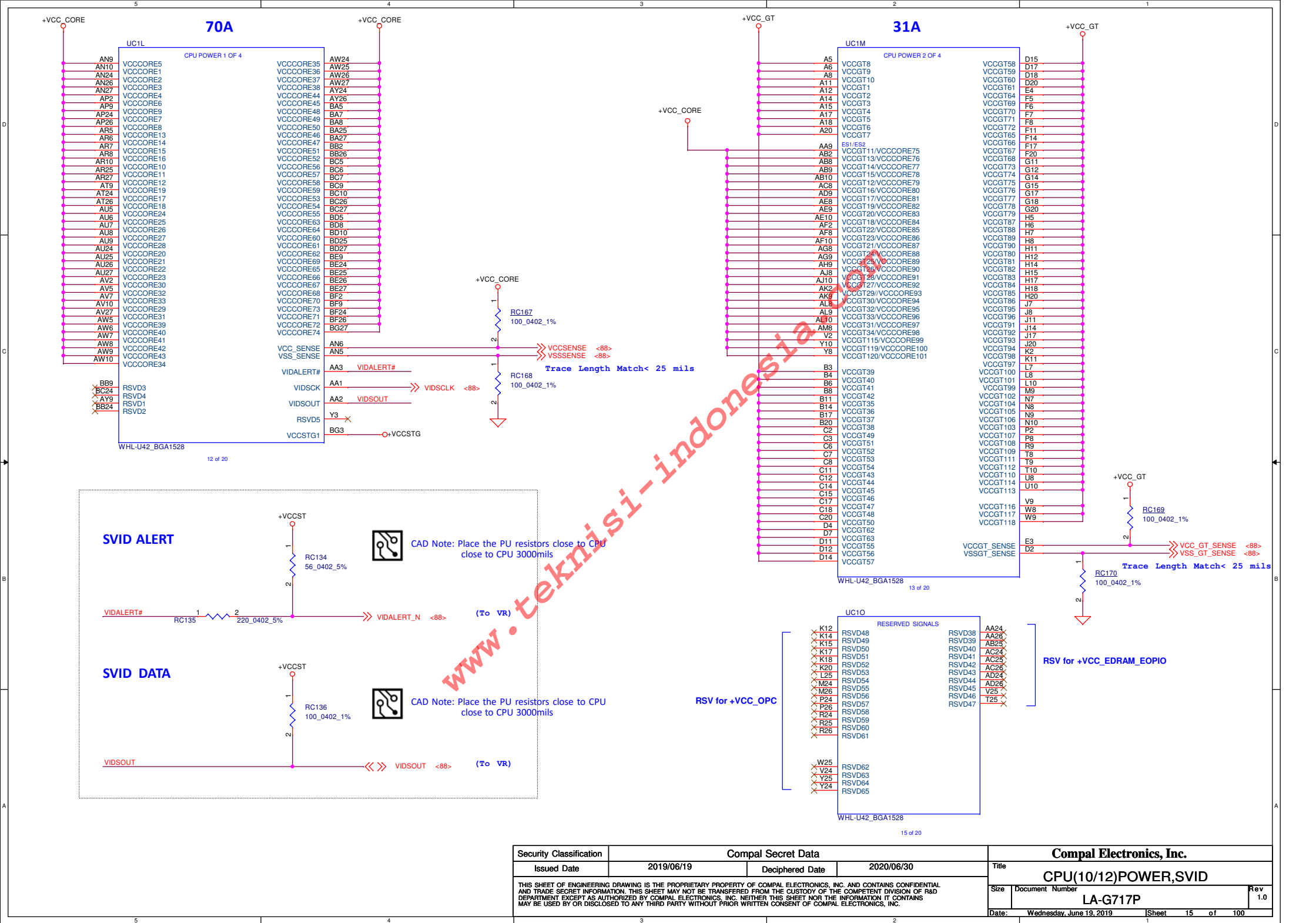
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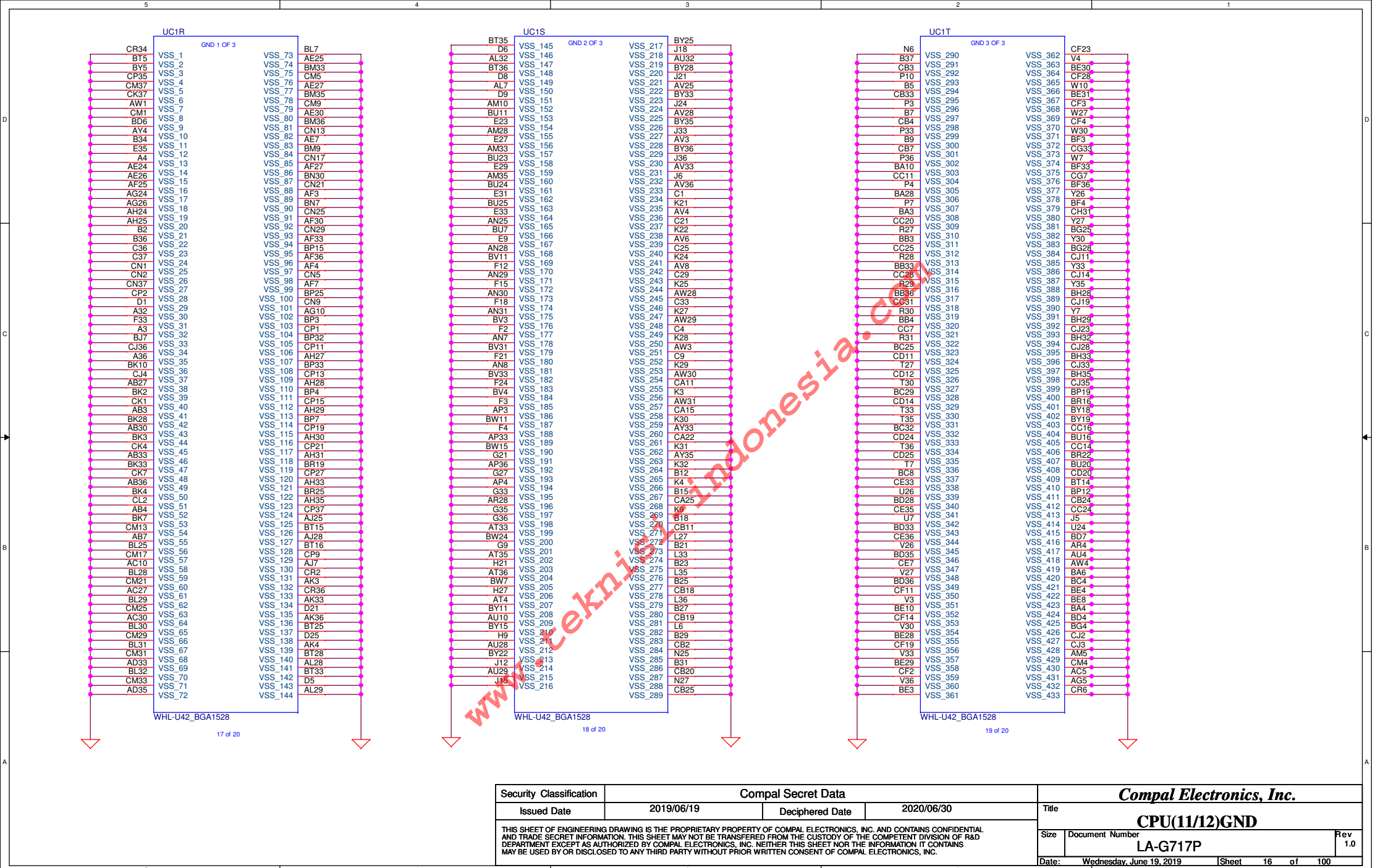


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		Size	Document Number						Rev
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		Date:	Wednesday, June 19, 2019			Sheet	16	of	100

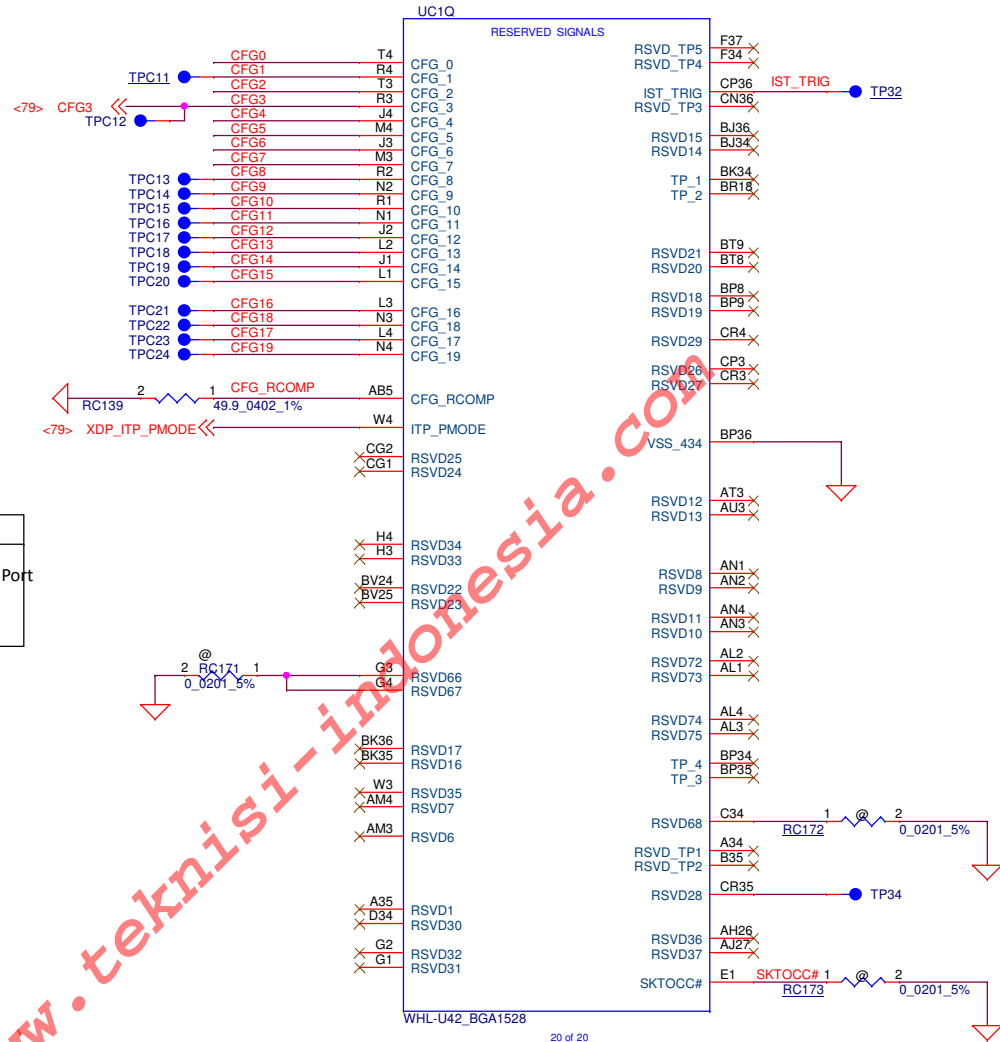
Reset sequence after PCU PLL is locked	
CFG0	1 : (DEFAULT) Normal Operation No Stall 0 : Stall

PCI Express Static Lane Reversal For All PEG Ports	
CFG2	1 : (DEFAULT) Normal Operation 0 : Lane Reversal

Display Port Presence Strap	
CFG4	0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	1 : Disabled; No Physical Display Port attached to Embedded Display Port

PCI Express Bifurcation	
CFG[6:5]	— 00 = 1x8 2x4 PCI Express* — 01 = reserved — 10 = 2x8 PCI Express* — 11 = 1x16 PCI Express*

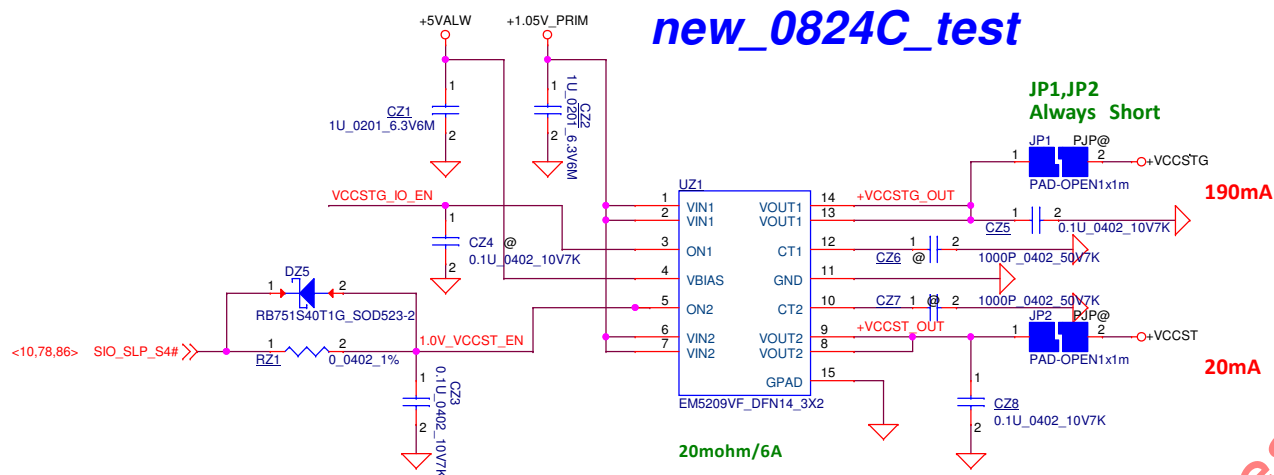
PEG Training	
CFG7	1 : (default) PEG Train immediately following RESET# de-assertion 0 : PEG Wait for BIOS for training.



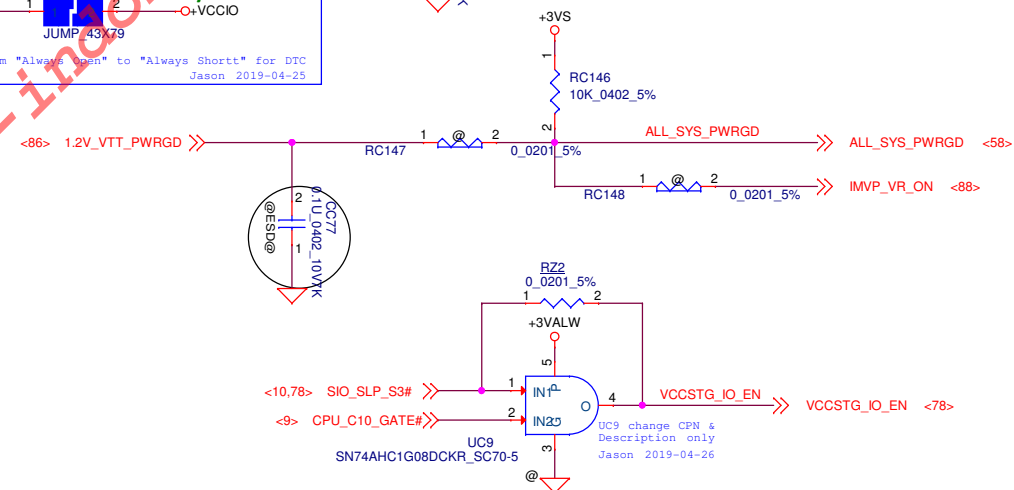
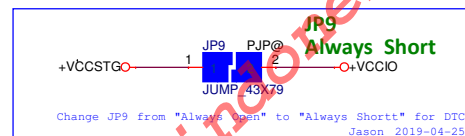
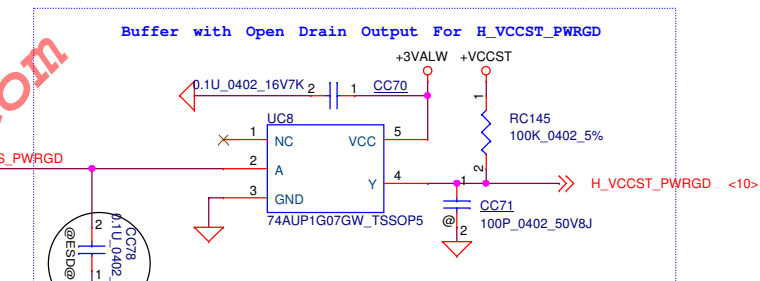
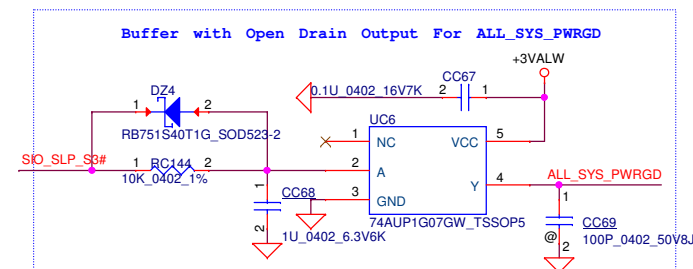
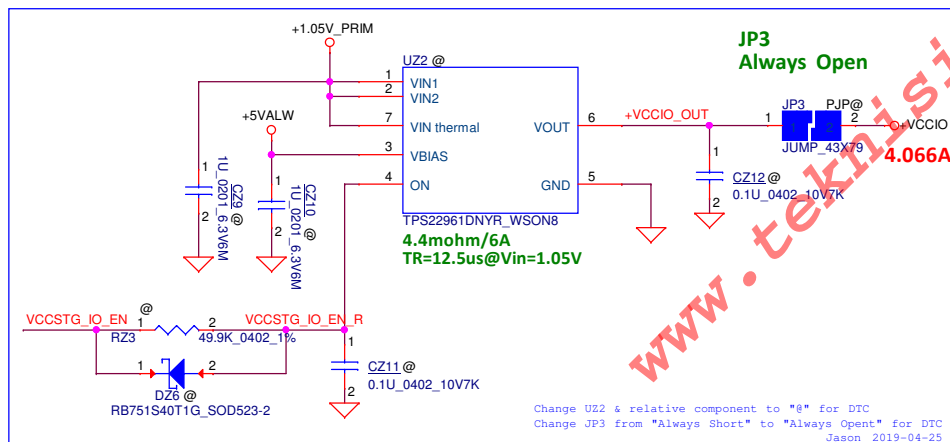
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+1.05V_PRIM TO +VCCST/+VCCSTG

new_0824C_test



+1.05V_PRIM TO +VCCIO



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						Size	Document Number				Rev
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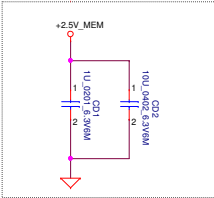
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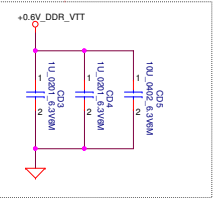
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Main Func = DDR

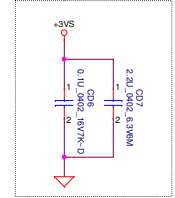
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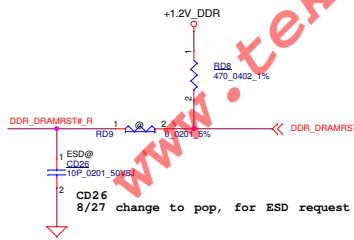
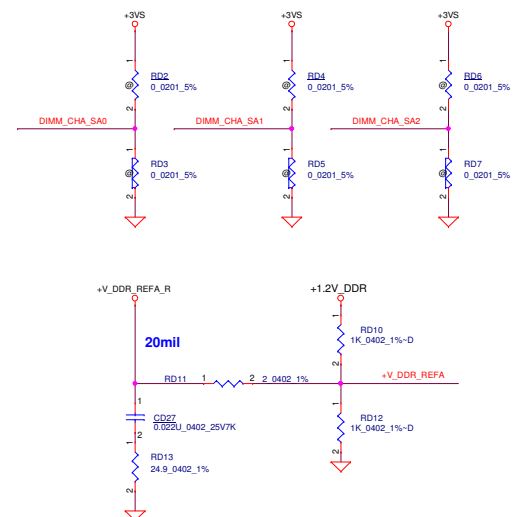
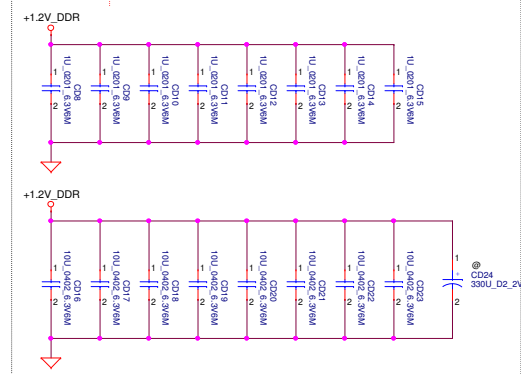
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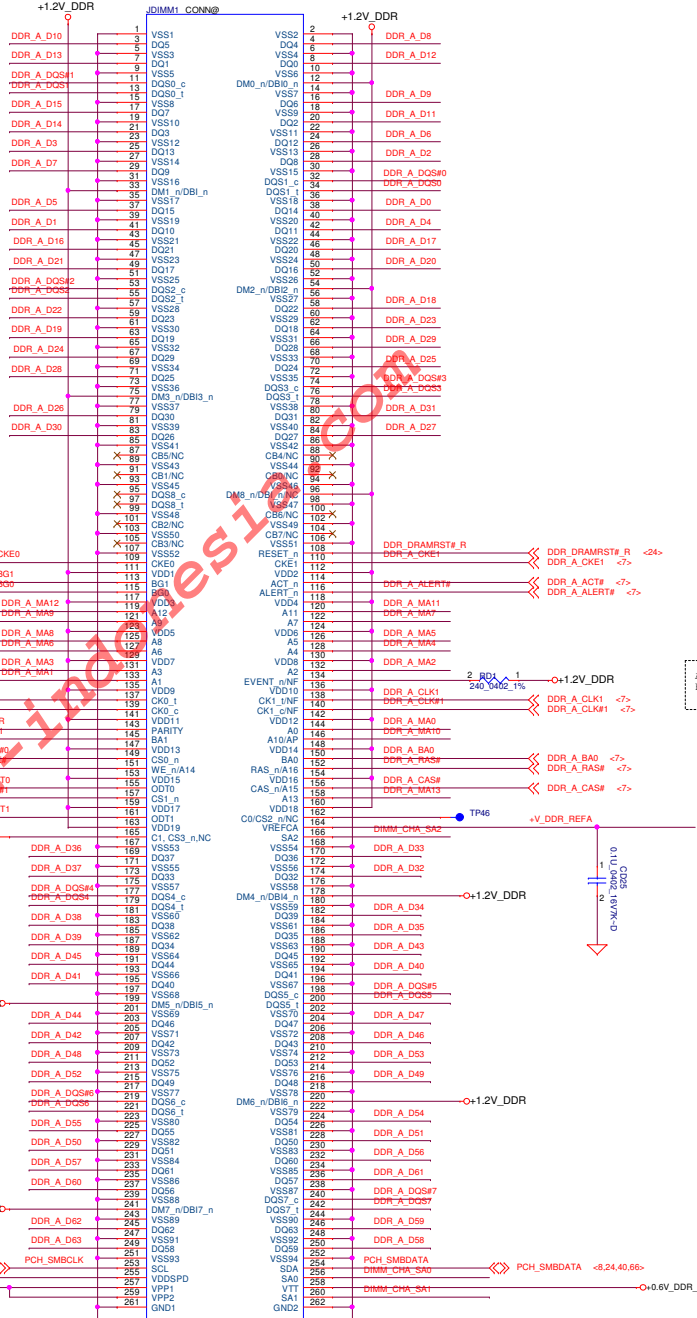
Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1



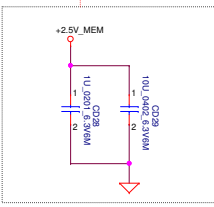
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<7> DDR_A_MA0..13
<7> DDR_A_DQ3#0..7
<7> DDR_A_DQ3#0..7



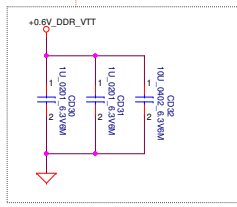
All VREF traces should
have 10 mil trace width

Main Func = DDR

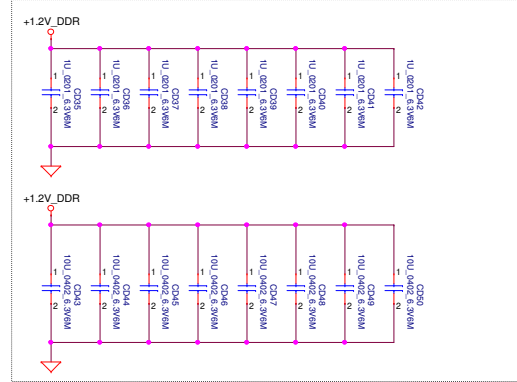
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Layout Note:
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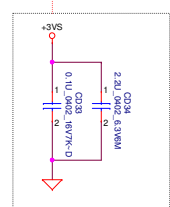


Layout Note:
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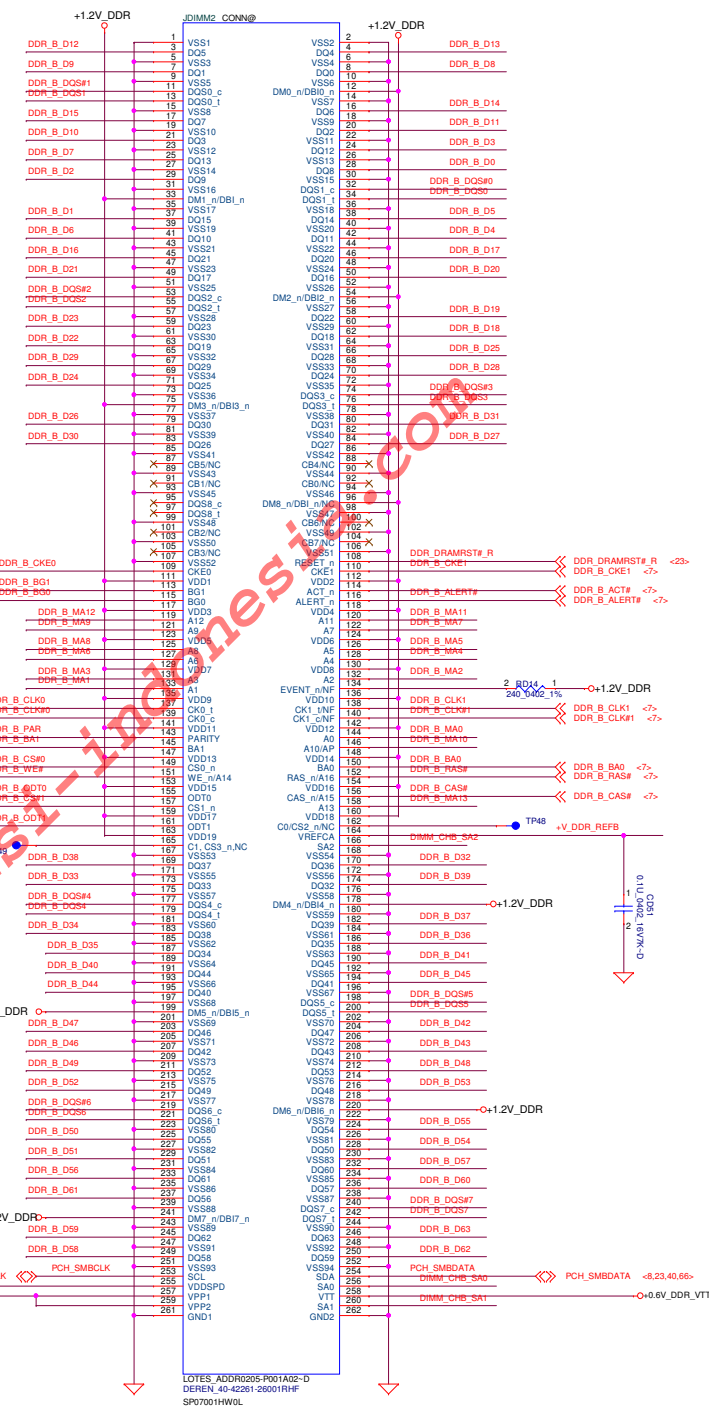
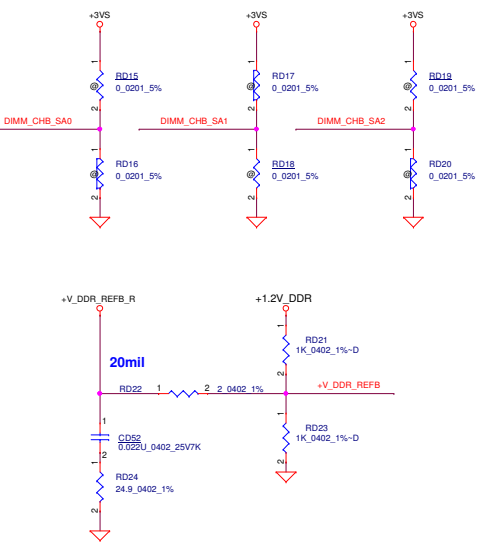


<7> DDR_B_D0[0..3]
<7> DDR_B_MA0[13]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS[0..7]

Layout Note:
Place near JDIMM2.255



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All VREF traces should
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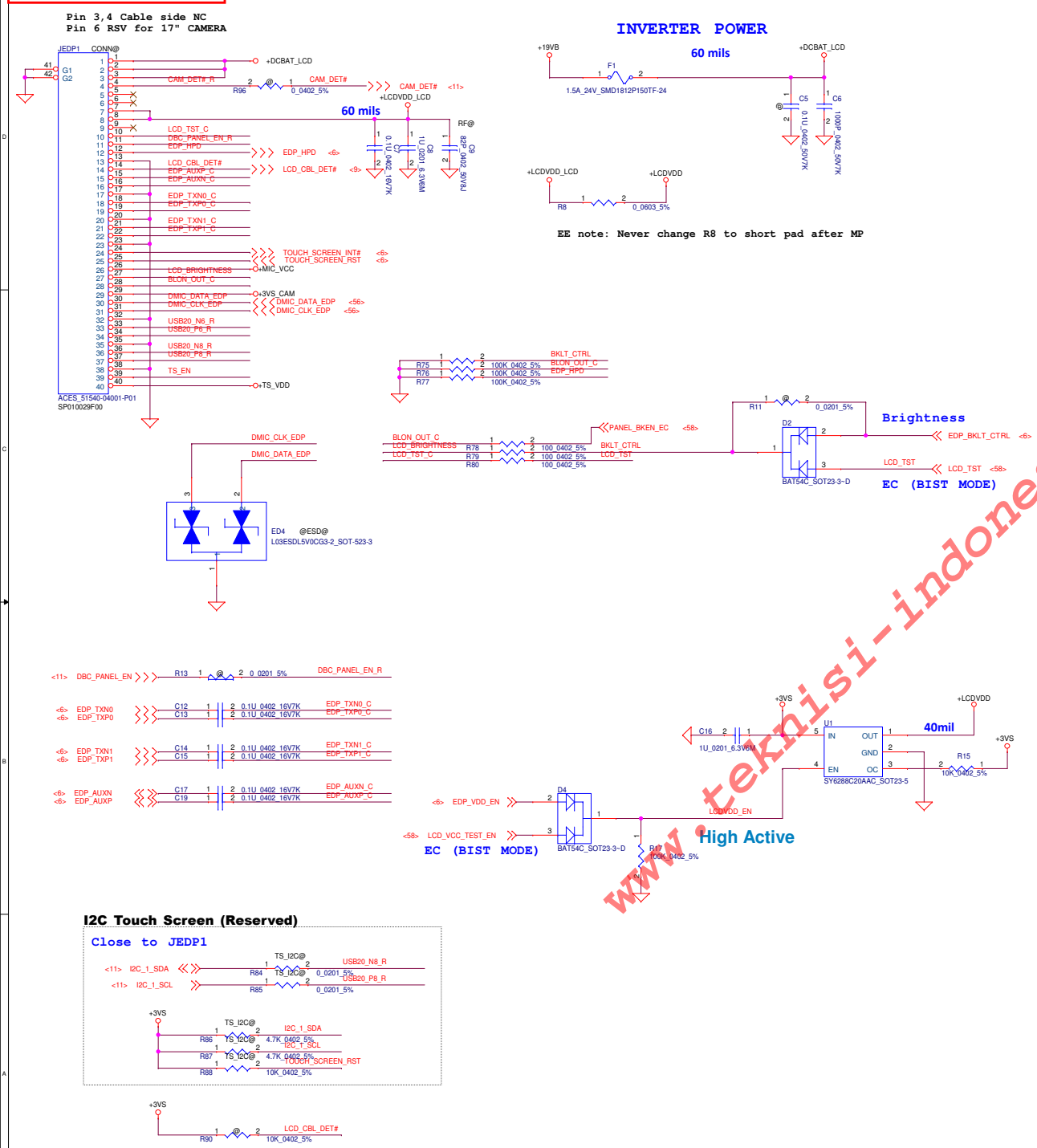
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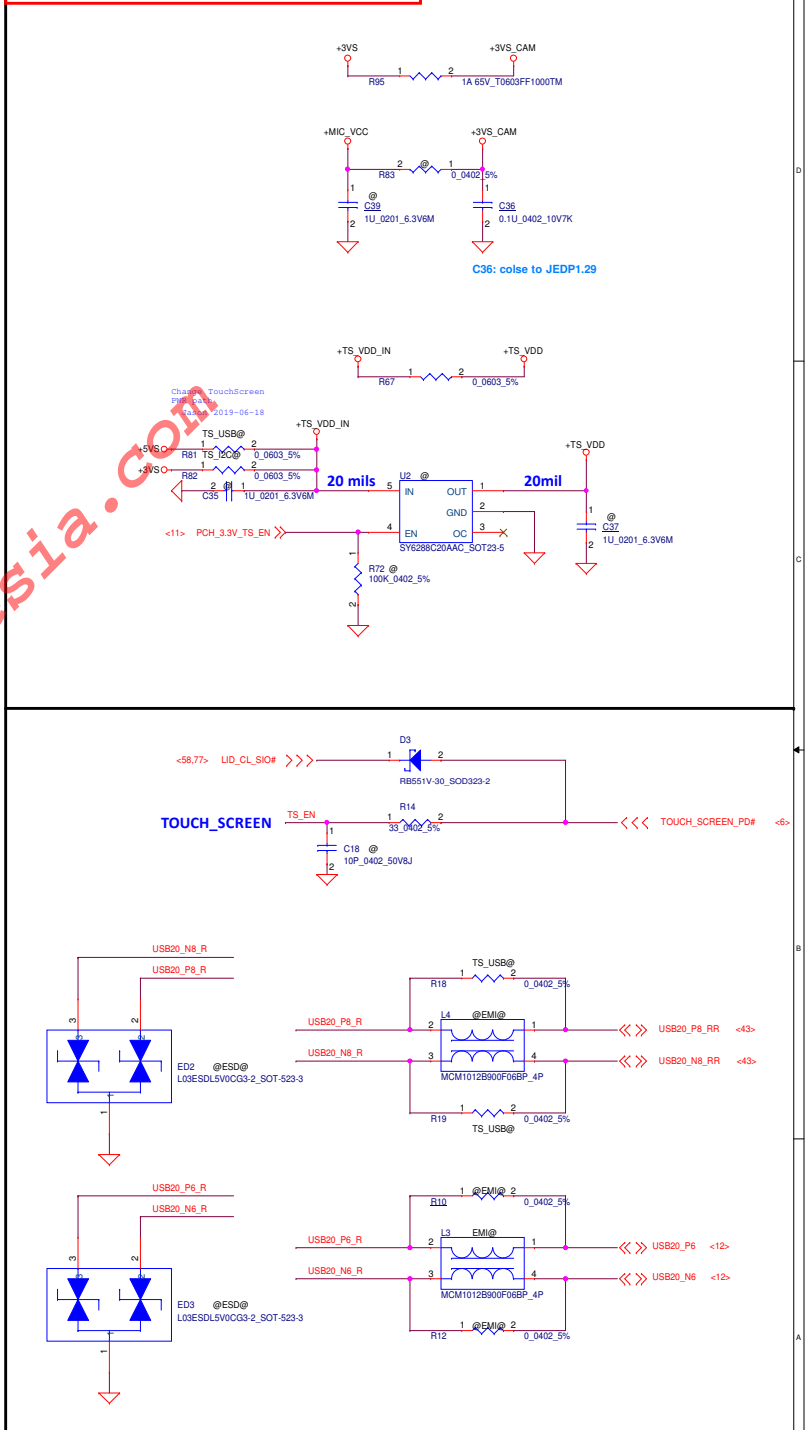
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Main Func = LCD



Main Func = CAM&MIC, TS



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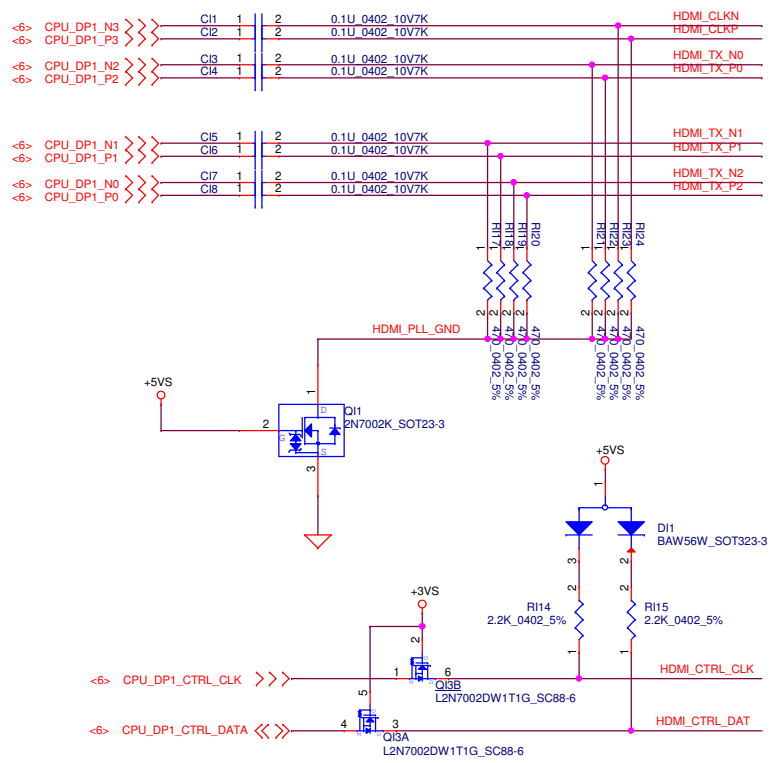
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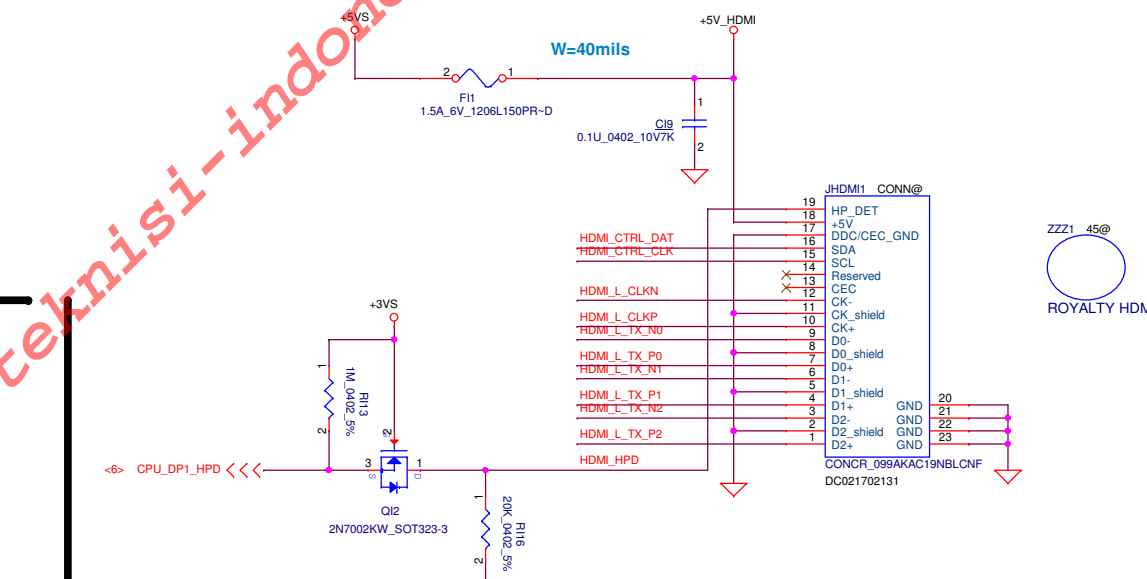
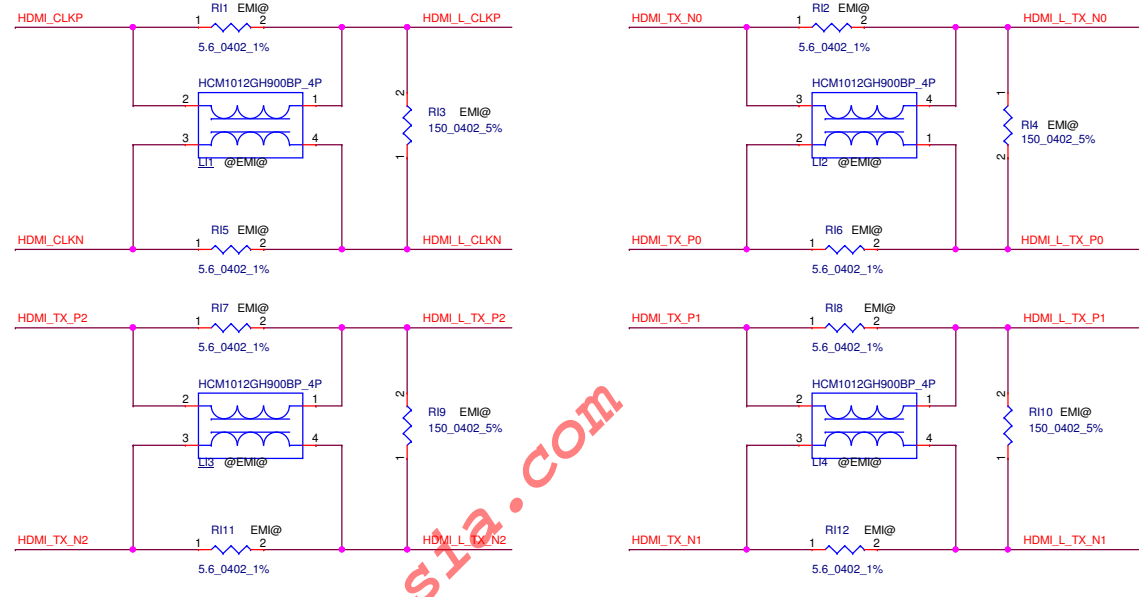
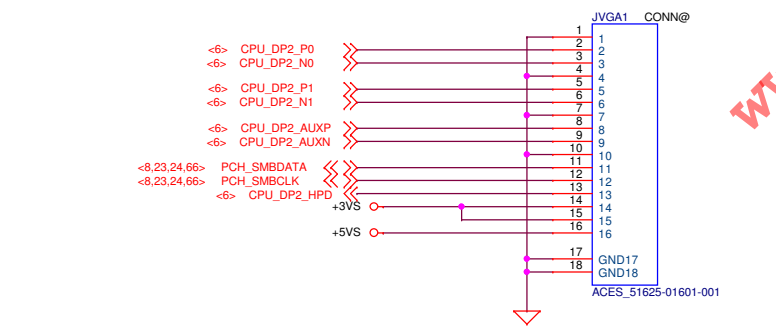
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Main Func = HDMI



Main Func = VGA



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										HDMI1.4	
										Size	
										Document Number	
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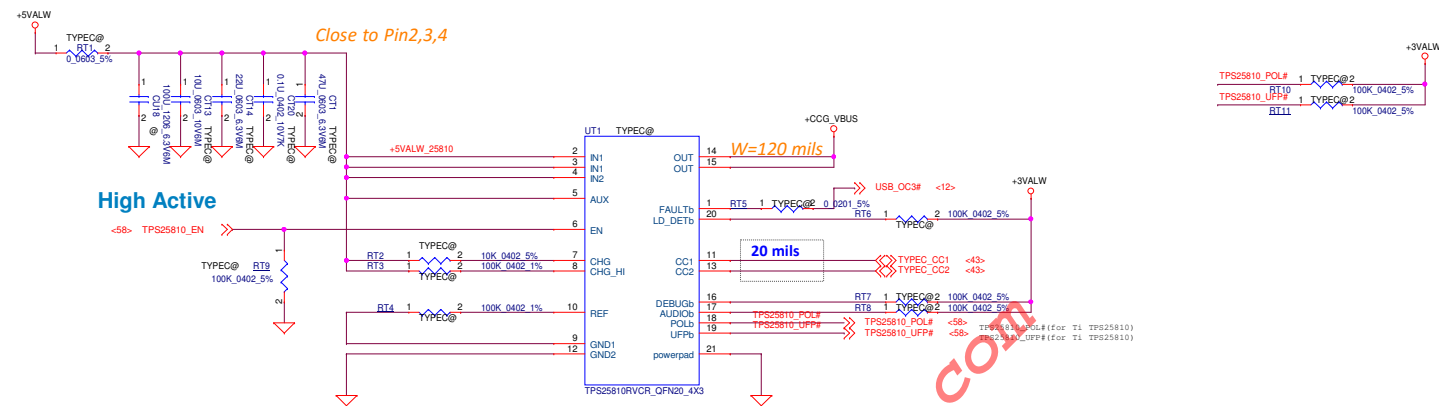
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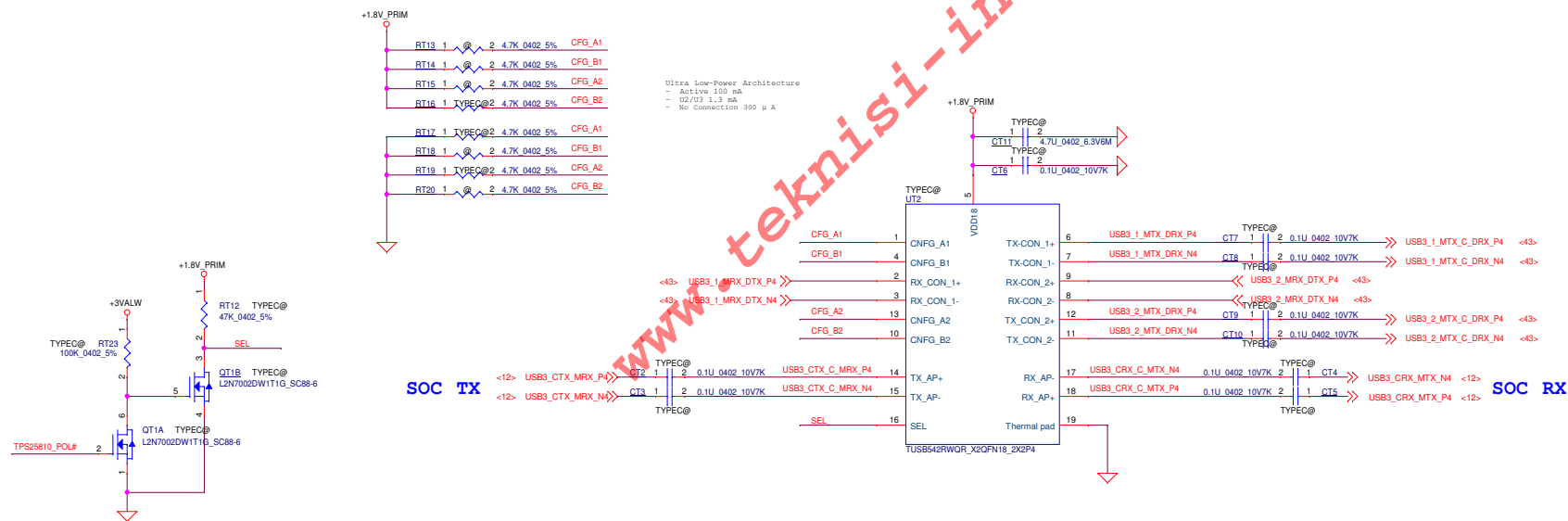
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Main Func = Power Switch

5V@3A



Main Func = Typec MUX



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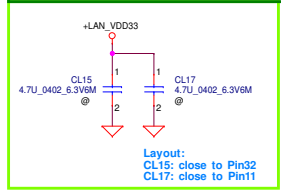
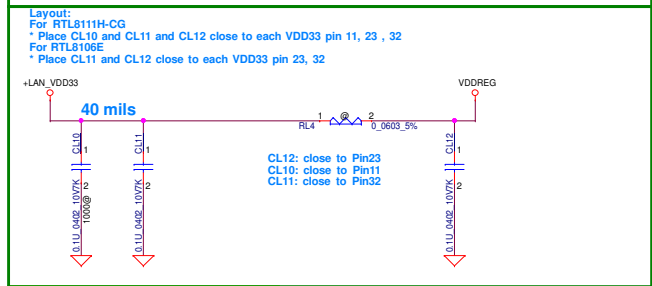
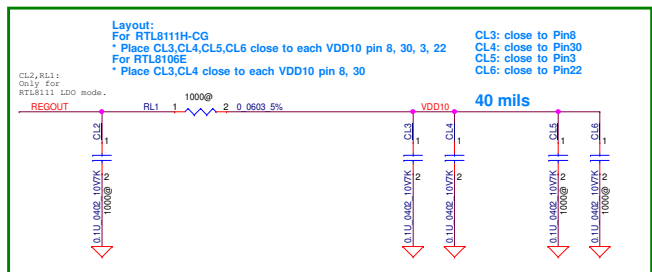
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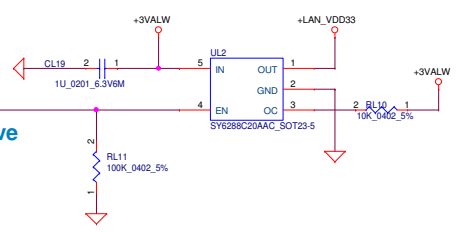
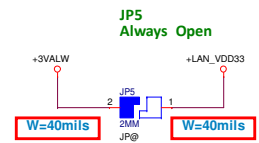
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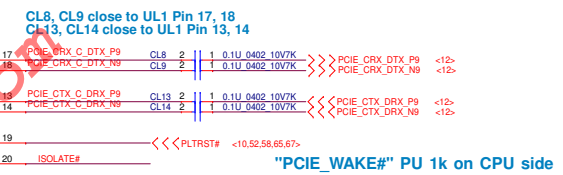
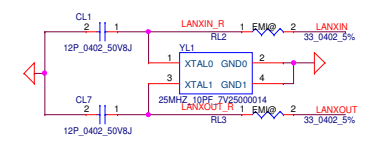
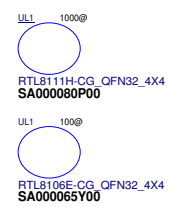
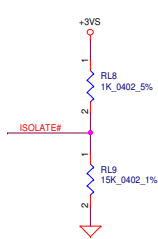


+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

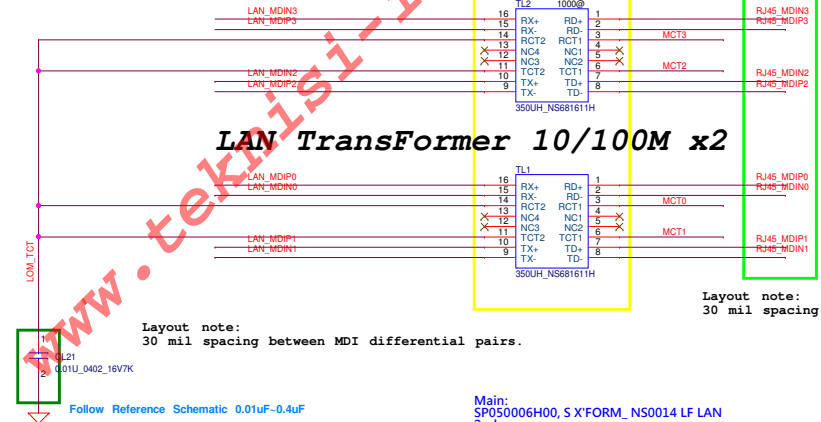


LAN CHIP 10/100/1000

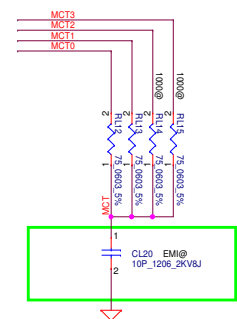
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LDO mode	LDO mode
10/100/1000M	10/100M



LAN TransForm 10/100M x2



TL1 TOP, TL2 BOT



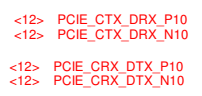
Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.

Main:
SP050006H00, S X'FORM_NS0014 LF LAN
2nd:
SP050006W00, S X'FORM_PD-245 10/100 PC CARD LAN

	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Main Func = WLAN



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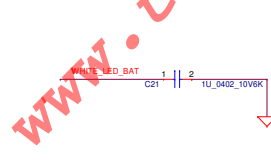
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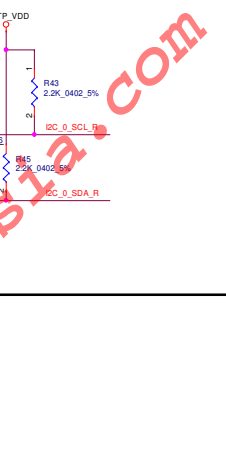
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Main Func = Battery LED



Main Func = TPAD



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			Size	Document Number LA-6717P
			Date	Worksheet Rev. 1.0
			Version	2019-06-19
			Sheet	60 of 100

Main Function:

Reserved

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				LA-G717P	
				Date:	Wednesday, June 19, 2019
				Sheet	63 of 100
				Rev	1.0

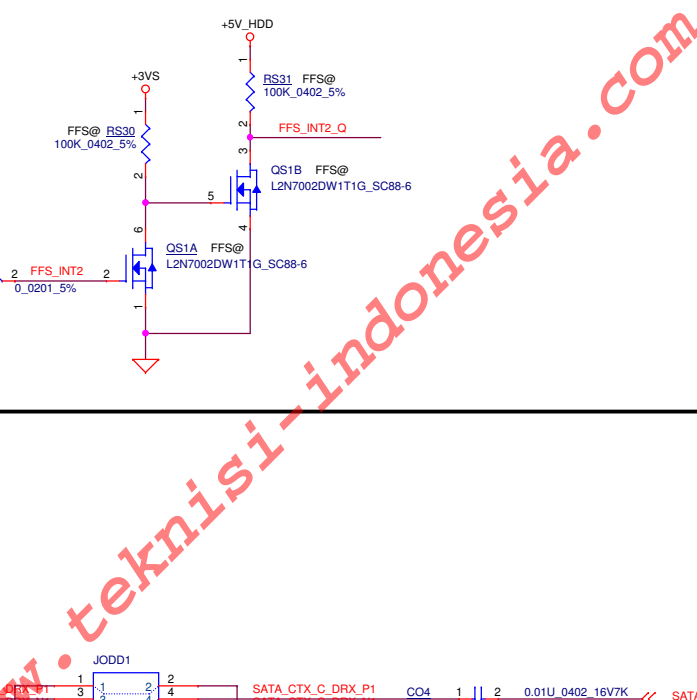
Main Function:

Reserved

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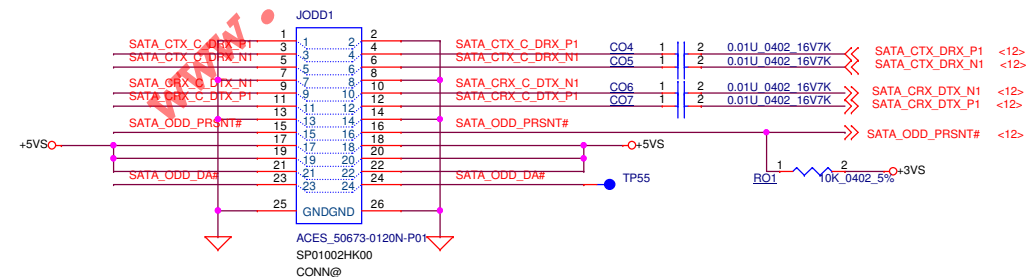
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Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	
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Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

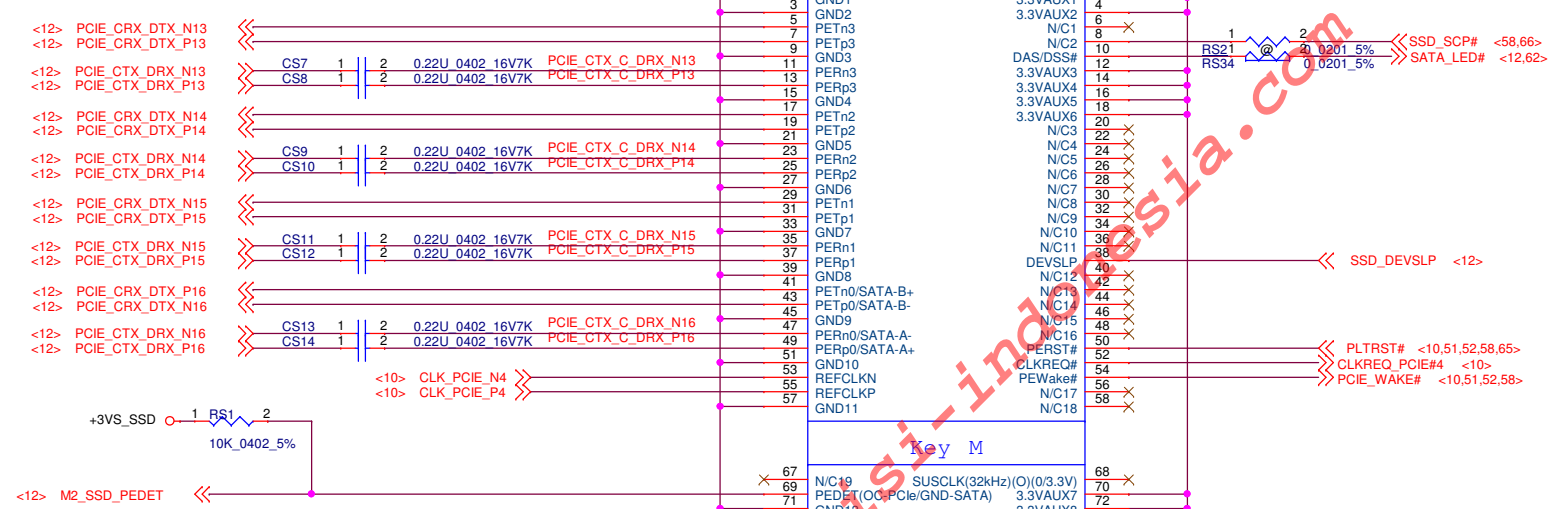
Main Func = ODD



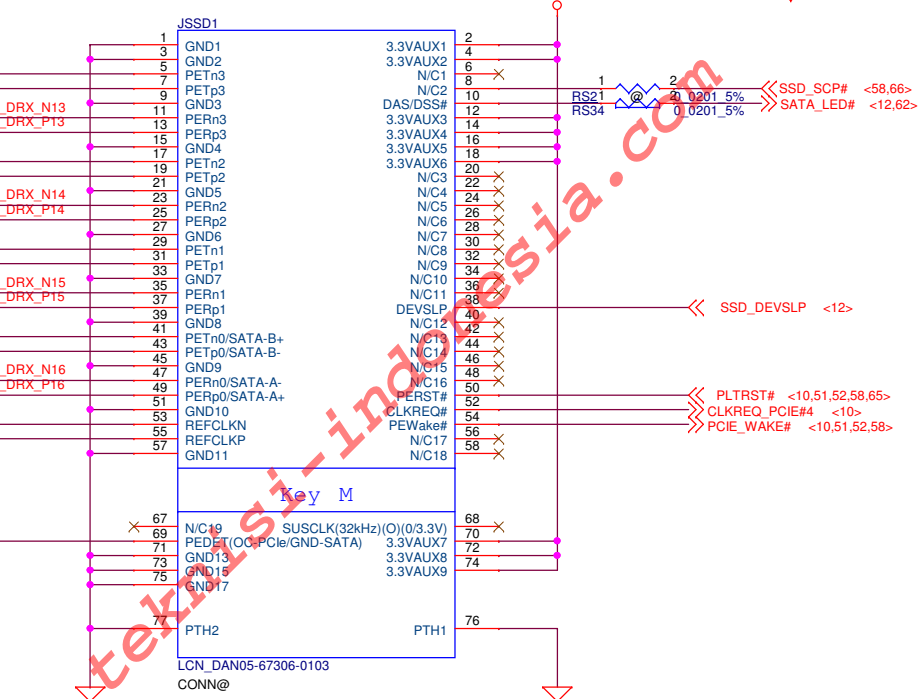
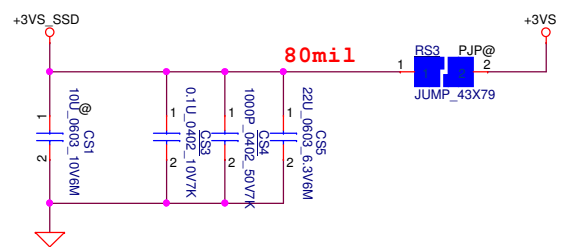
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9 10 11
5V	P3	
At t e n t i o	P4	12
GND	P5	
GND	P6	

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				Custom	LA-G717P Rev 1.0
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NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE



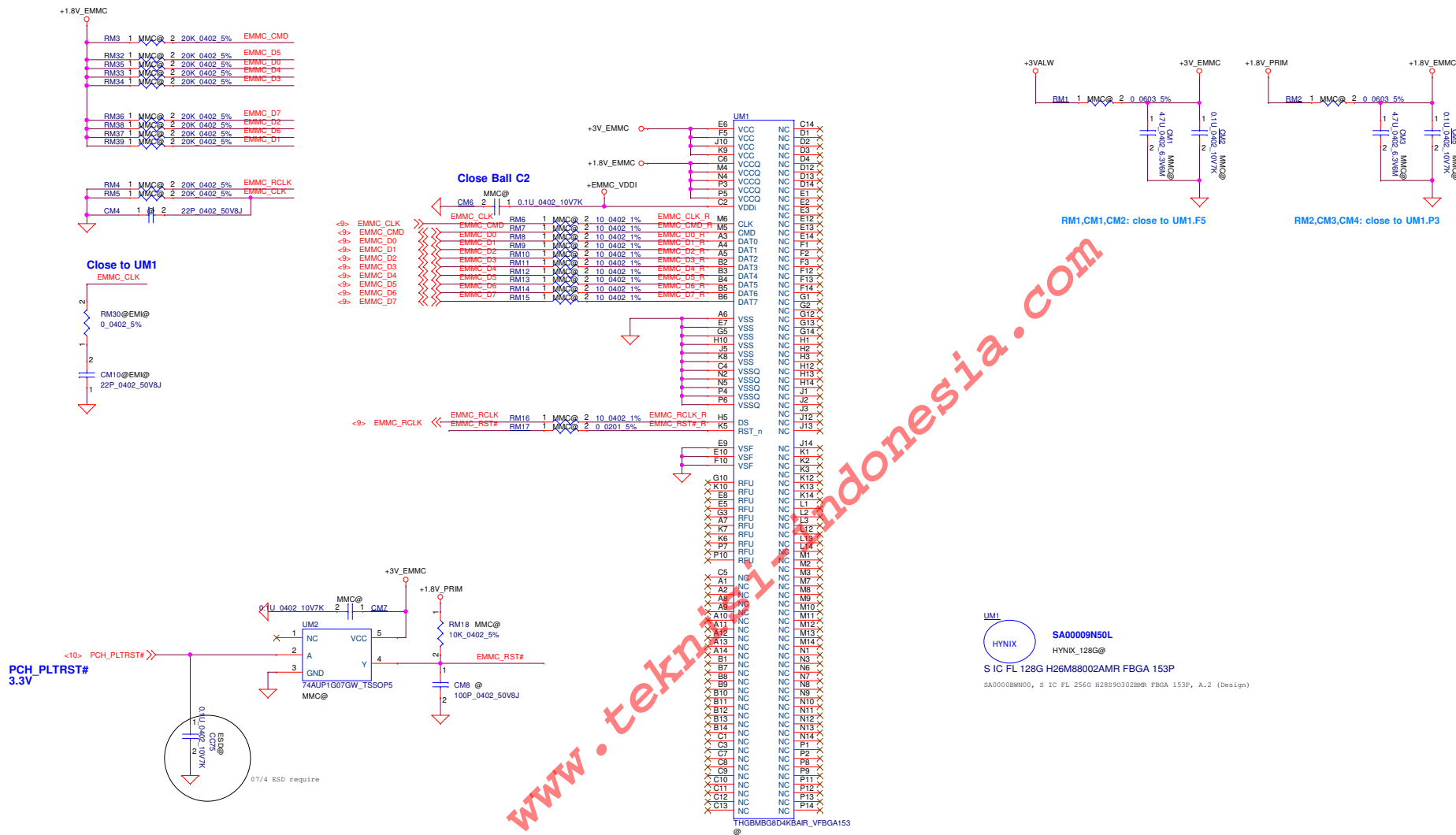
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Main Func = eMMC



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				Rev 1.0
				LA-G717P
				Date: Wednesday, June 19, 2019
				Sheet 69 of 100

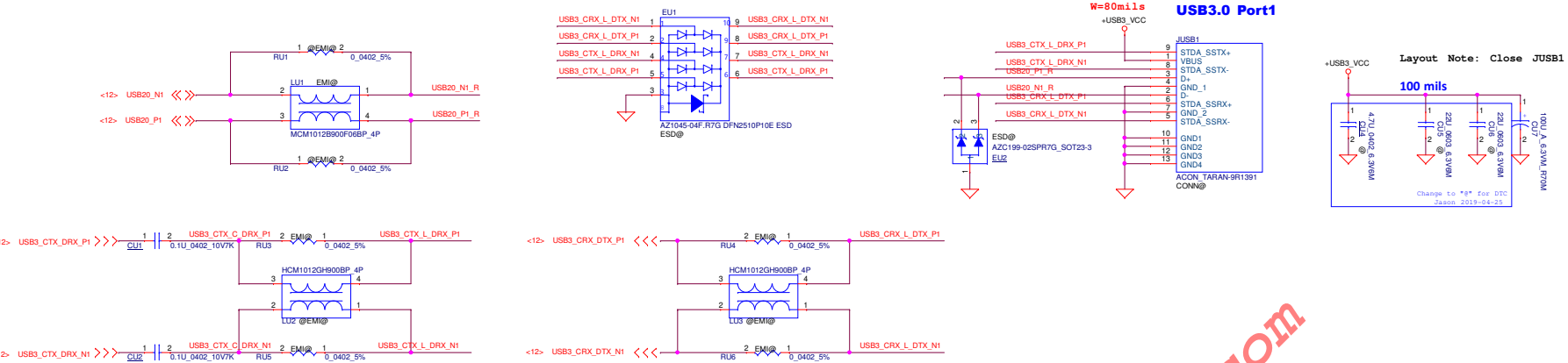
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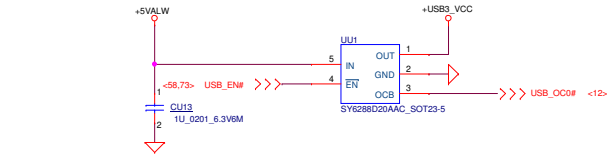
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				Document Number	1.0
				LA-G717P	
				Date:	Wednesday, June 19, 2019
				Sheet	70 of 100

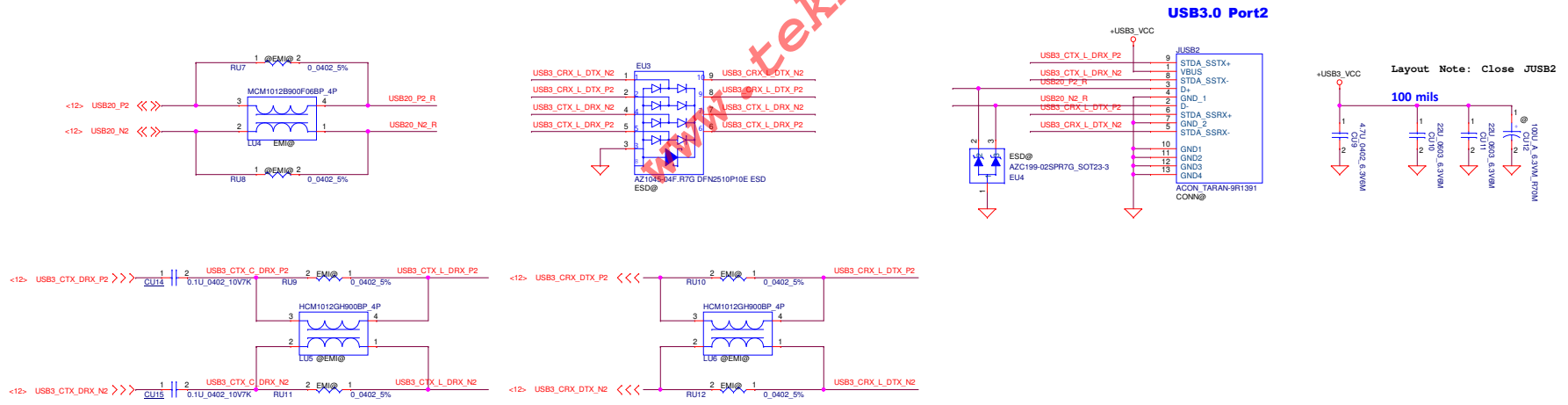
Main Func = USB3.0 Port1



Maximum Output Current 2A



Main Func = USB3.0 Port2



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Size	Document	Number	LA-G717P	Rev 1.0
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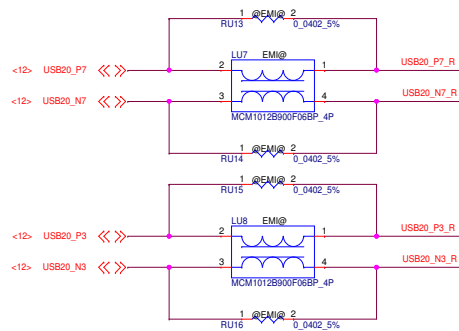
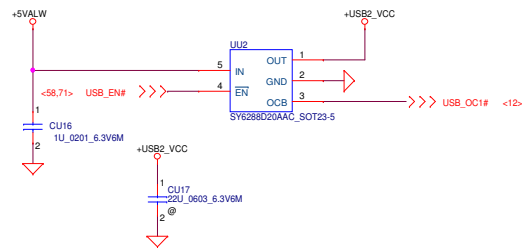
Main Function:

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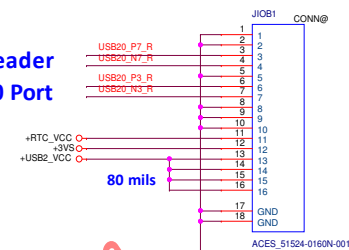
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				Size	Rev
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Main Func = USB2.0 Port3 + Card Reader on IO/B



USB2.0/Card Reader connector

CardReader
USB2.0 Port



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					LA-C717P	1.0
				Date:	Wednesday, June 18, 2019	Sheet 73 of 100

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				Document Number	1.0
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				LA-G717P	
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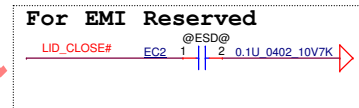
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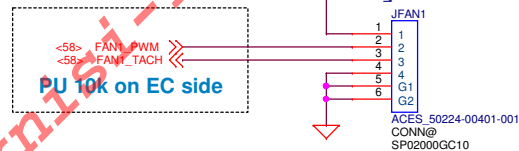
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Low activated from KBC GPIO

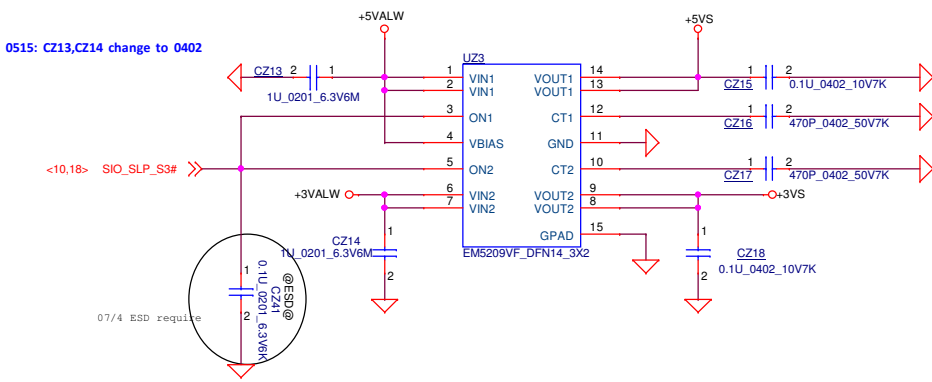


FAN

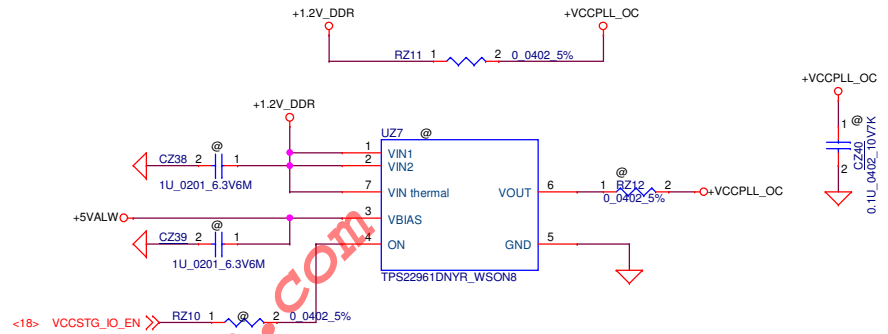


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				LA-G717P	
				Date: Wednesday, June 19, 2019	Sheet 77 of 100
				Rev	1.0

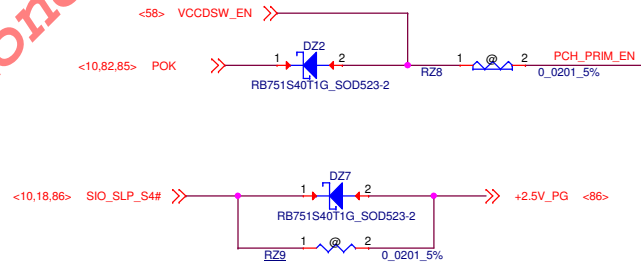
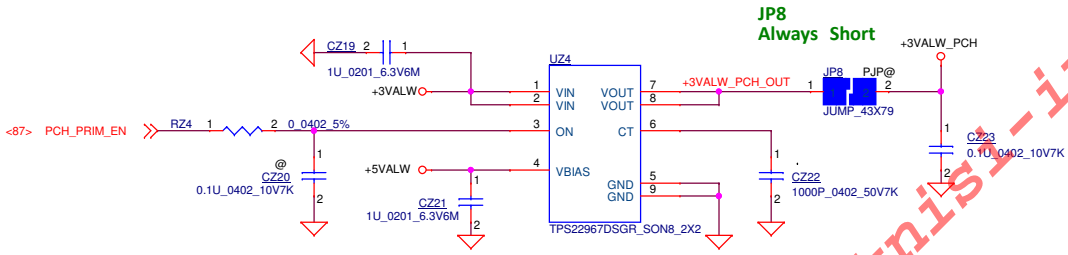
+5VS/+3VS for System



+VCCPLL_OC source



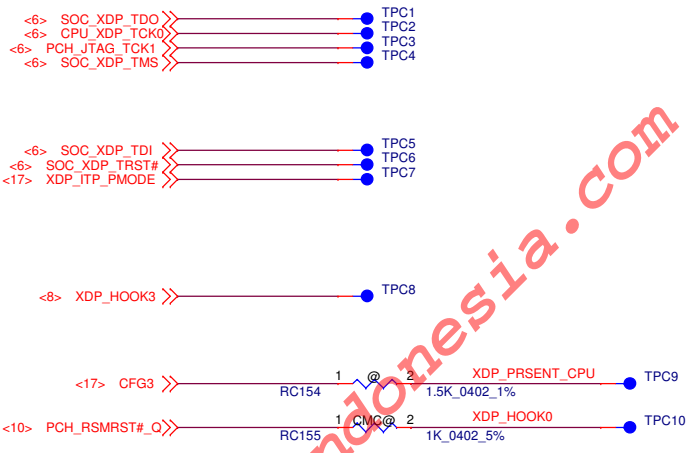
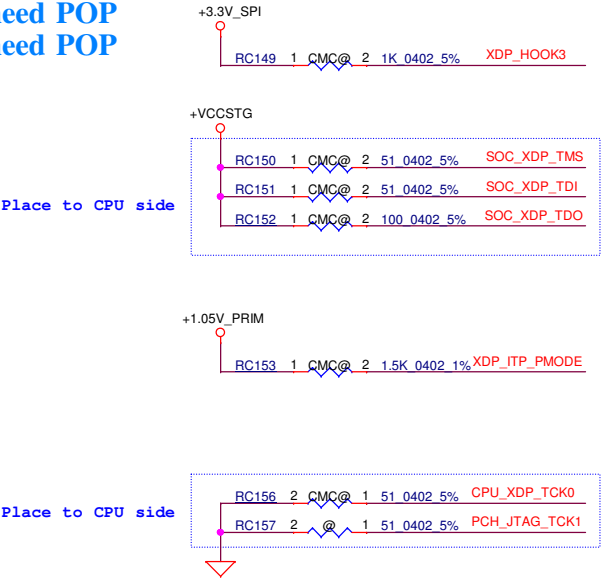
+3VALW_PCH for System



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PortConnector Less Routing Topology

Follow KBL DCI Link
RC152 need POP
RC156 need POP



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Main Func = Power Monitor


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Reserve

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Title		Reserve for PWR	
Size	Document Number		Rev 1.0
Date: Wednesday, June 19, 2019		Sheet 81 of	100

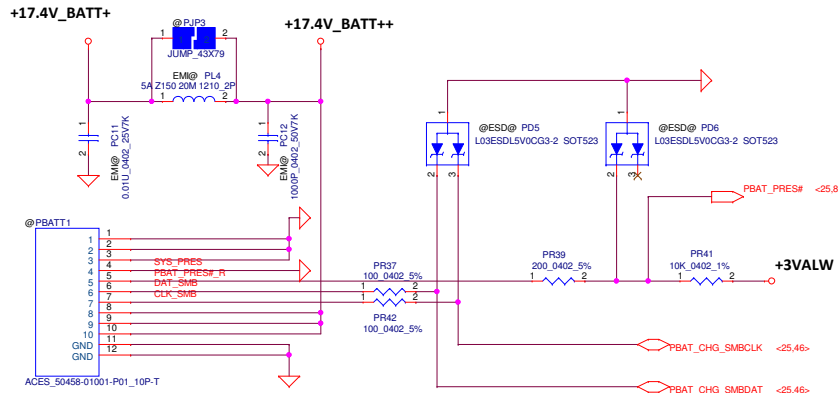
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Main Func = BATT CONN

Battery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T



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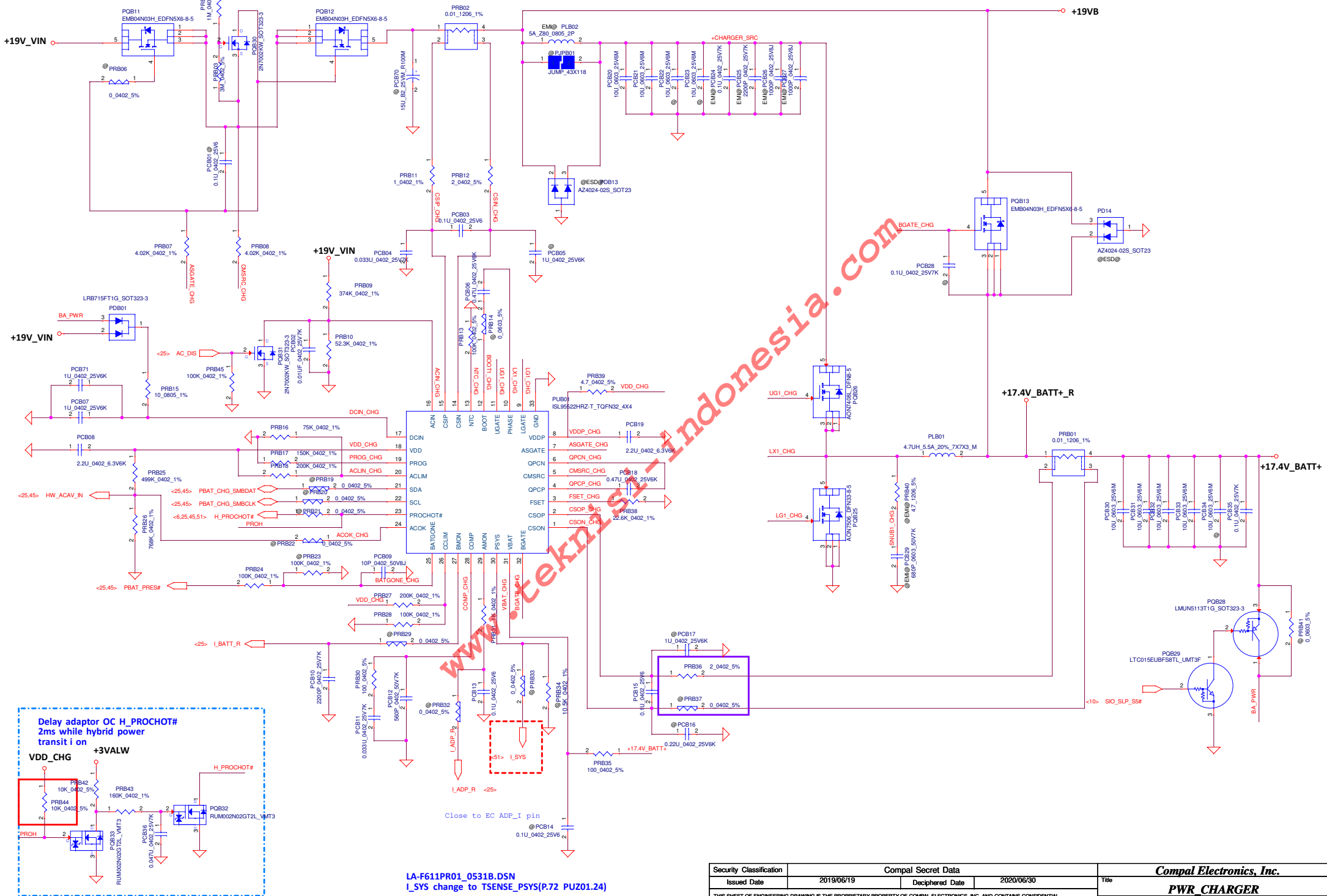
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PWR_BATT_CONN

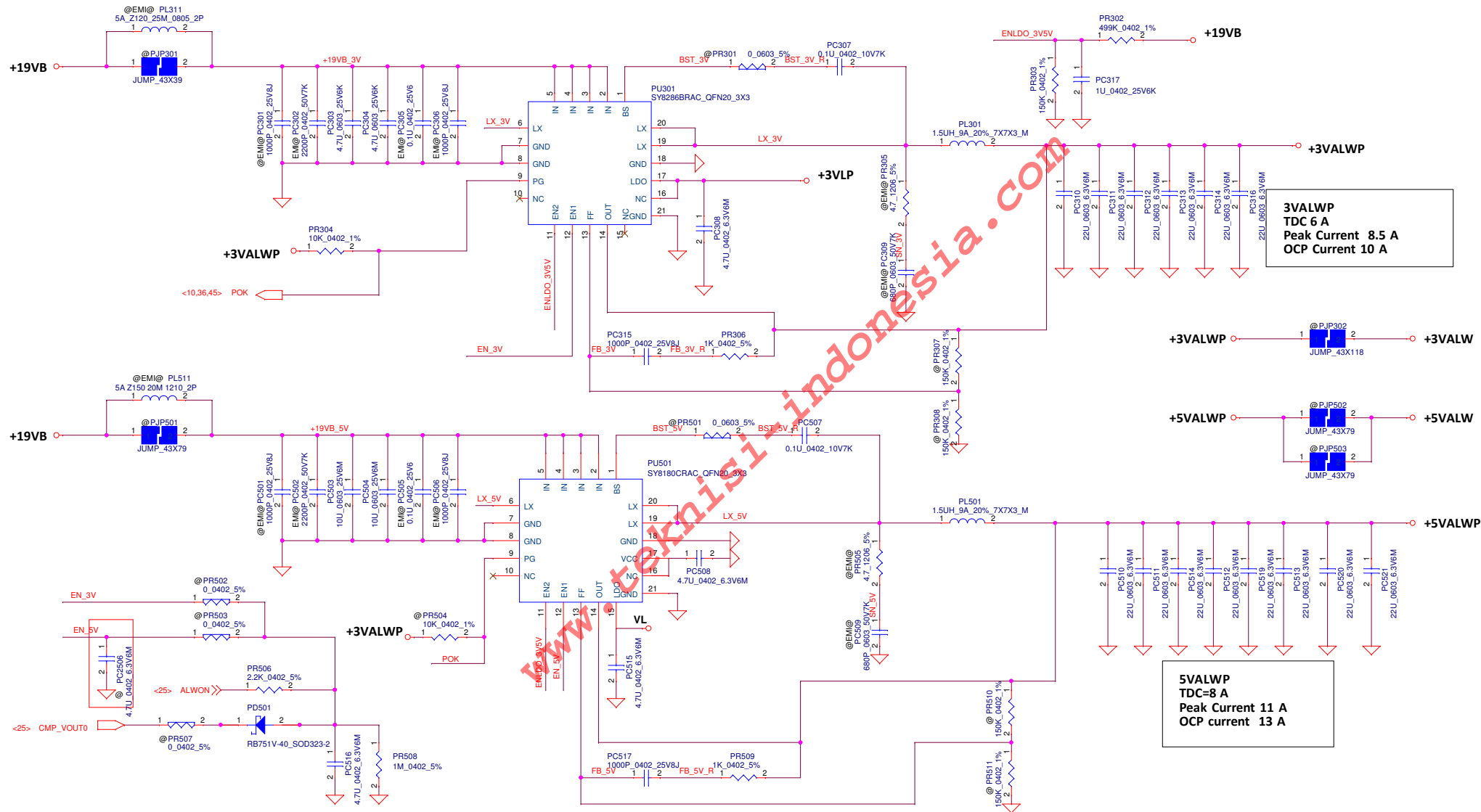
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Main Func = CHARGER



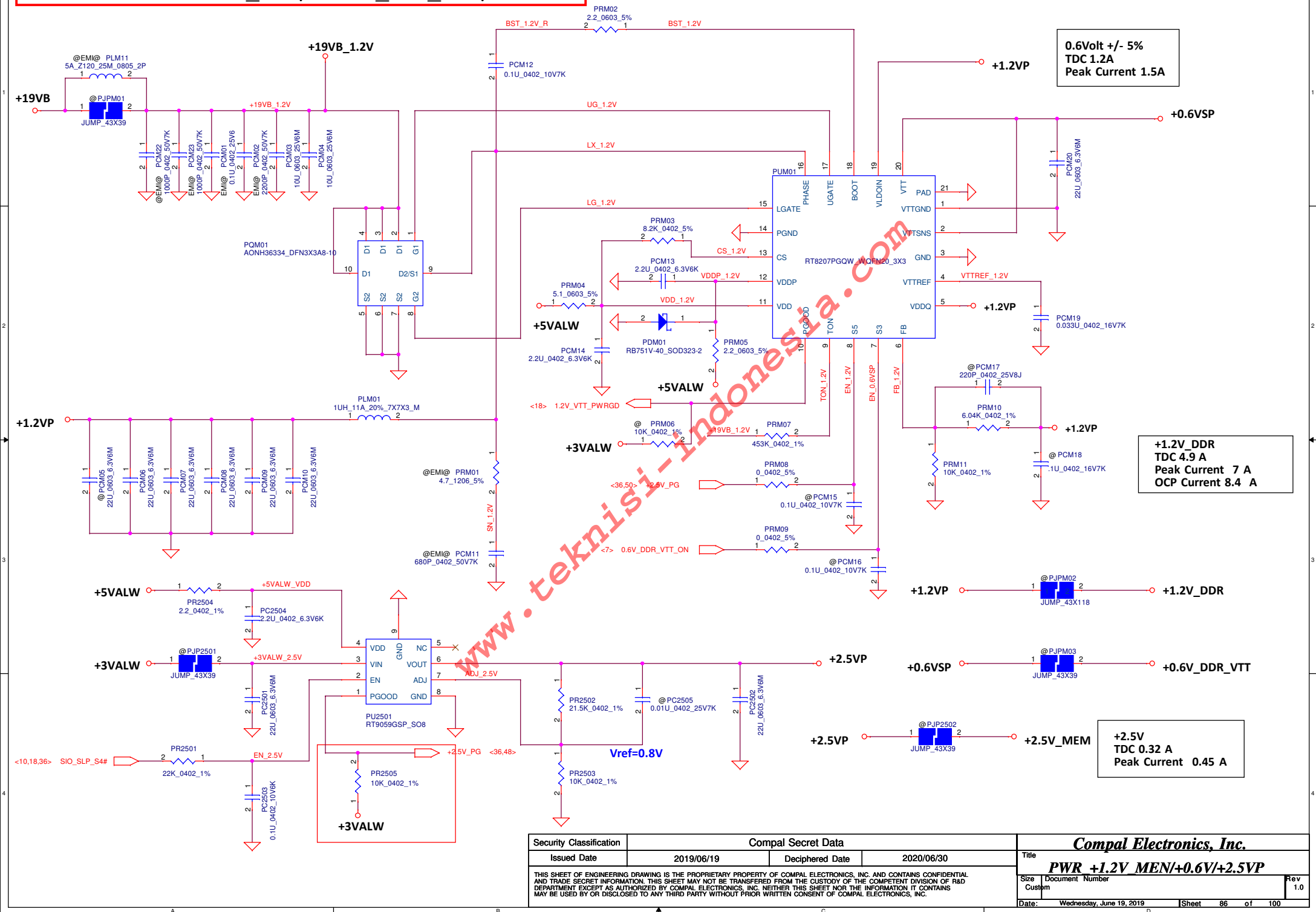
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Main Func = 3.3VALWP/5VALWP

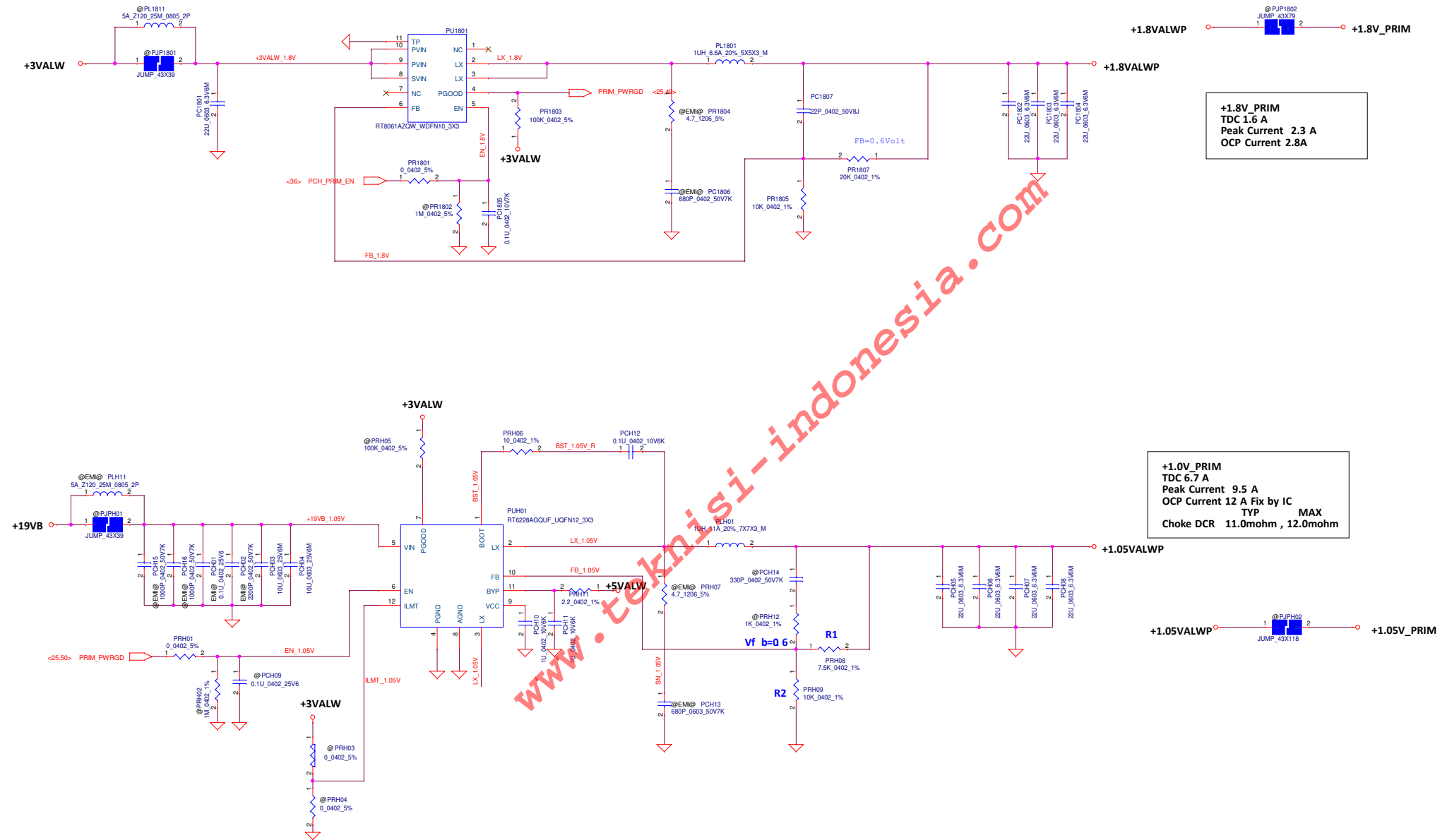


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				Size	Document Number	Rev
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/ +2.5VP

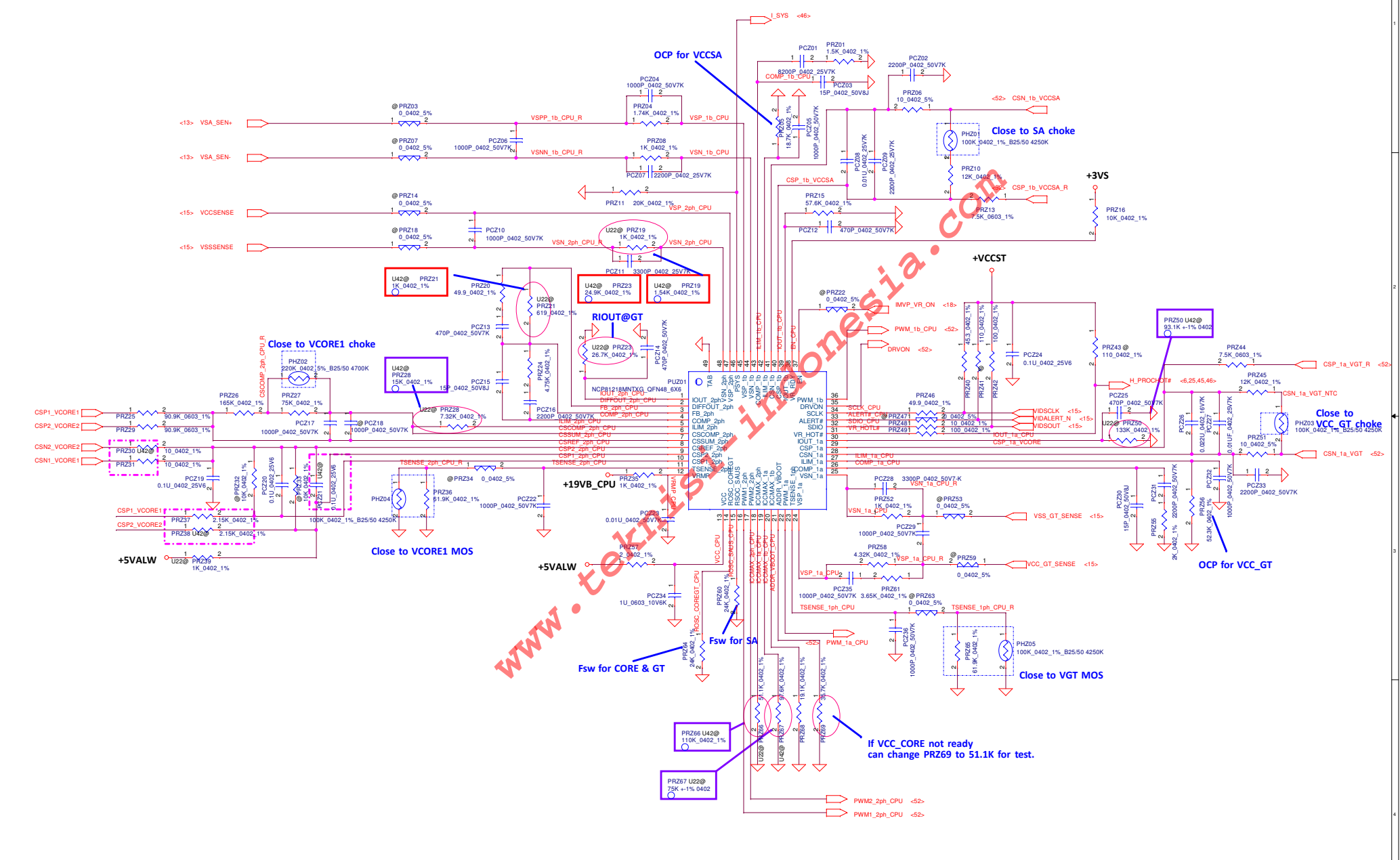


Main Func = +1.8VALWP / +1.05VALWP



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Main Func = CPU



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VCCGT_B+

5A Z150 20M 1210_2P

330uF 20V 1608

VCCGT

0.15uH NA_36A_20%

VCCGT_B+

VCCGT

U22 - 15W

Loadline : 3.1m-ohm

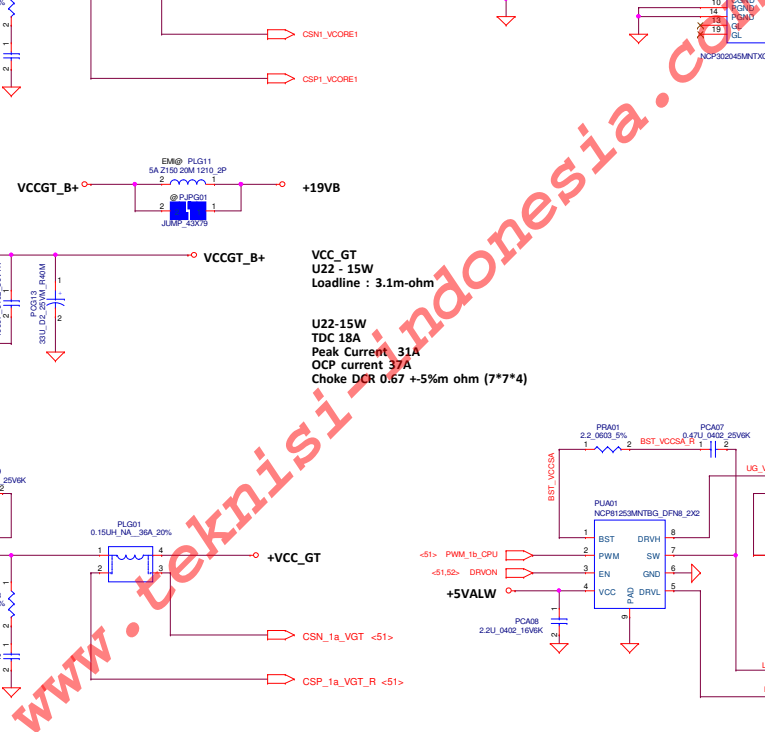
U22-15W

TDC 18A

Peak Current 31A

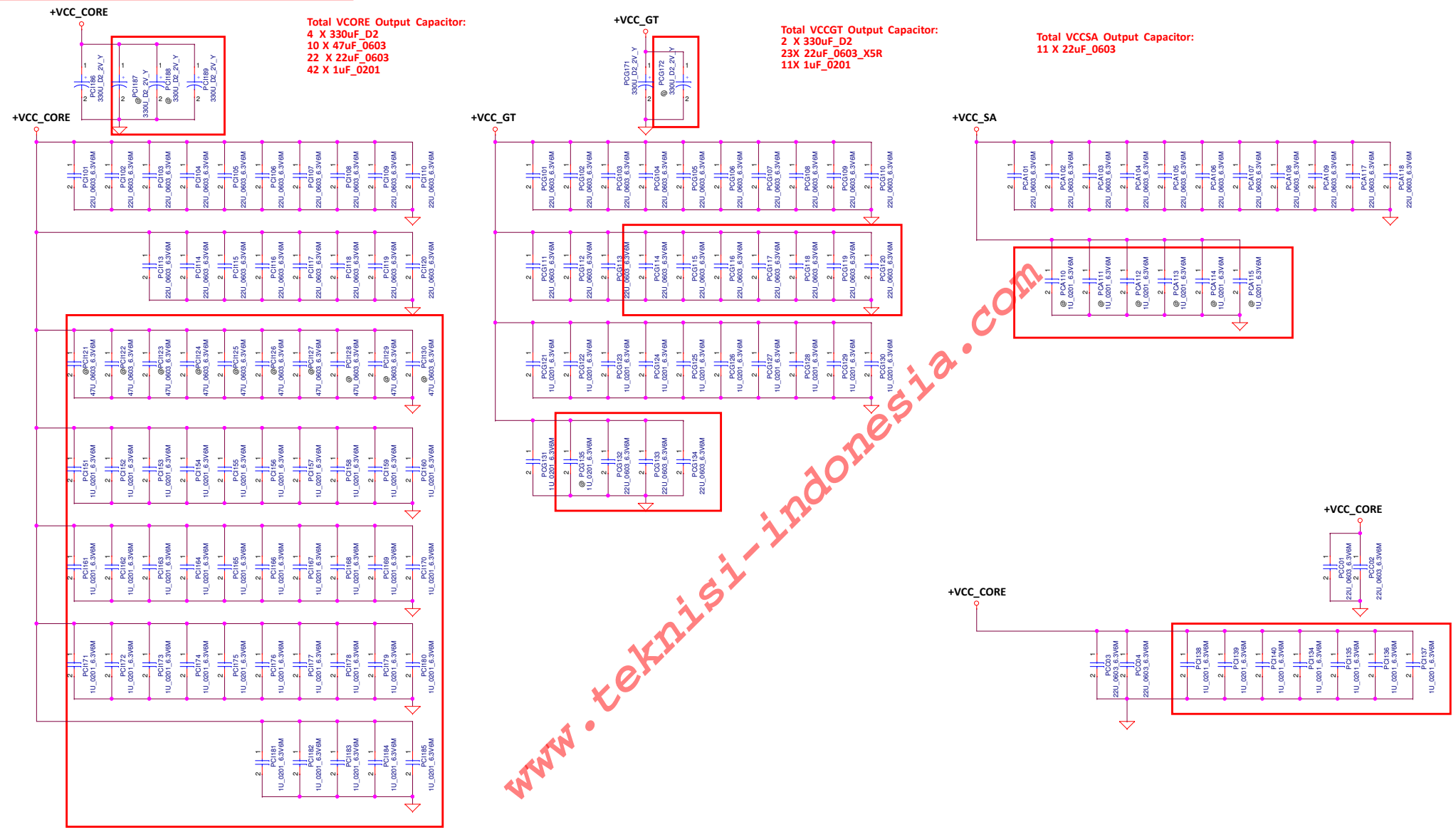
OCF current 37A

Choke DCR 0.67 +5% m ohm (7*74)



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Main Func = CPU / VGA / SA MLCC



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Version Change List (P. I. R. List)

DVT1 EE change list

Design Change					
Item	Date	Page	Part reference	Change description	Reason
Based on 05/15					
1	2018/5/17	8		Add RC207, CPU_SPI_0_CS#1	For 2nd ROM
2	2018/5/17	14		CC52,CC48,CC51,CS change to 0402	meet purchase requirement
3	2018/5/17	29		CV73*CV78, CV100*CV109 change to 0402	meet purchase requirement
4	2018/5/20			Del C56,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize
5	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch
6	2018/6/4	38		Connect UCL1.CC30 to R72, Add RC208,RC209	For 17" Touch
7	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize
8	2018/6/4	16		CL16 change to 0201	MLCC downsize
9	2018/6/13	56		CA16 change to 0402	MLCC downsize
10	2018/6/19	71		Swap D+/D- on JUSB1 Conn	For BITS377044
11	2018/6/19	38		Add LCD_CBI_DET# on Jedp pin14 and Connect to GPP_C10	For BITS378028
12	2018/7/4	65		add Rx10*14	co-lay ST TPM
13	2018/7/4			add CC75,C241,CC76,CC77,CC78,CC79	For ESD requirement
14	2018/7/6	65		add Rx15*RX19	co-lay China TPM

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1 (x00)
2	P56	PWR	20160321	COMPAL			0.1 (x00)
3							
4							
5							
6							
7							
8							